

Personal Daq/3000 Series

USB 1-MHz, 16-Bit Multifunction Modules

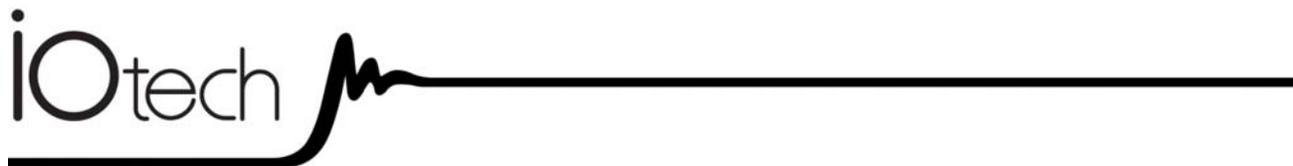
Requires a version of Windows[®]



Windows Vista (32 or 64-bit)
Windows XP SP2 (32-bit)
Windows 2000 SP4



Personal Daq/3000
Personal Daq/3001
Personal Daq/3005



Personal Daq/3000 Series

1136-0901 rev 2.1



372751-01

Measurement Computing

10 Commerce Way
Norton, MA 02766

(508) 946-5100

Fax: (508) 946-9500

info@mccdaq.com

www.mccdaq.com

Warranty Information

Contact Measurement Computing by phone, fax, or e-mail in regard to warranty-related issues:
Phone: (508) 946-5100, fax: (508) 946-9500, e-mail: info@mccdaq.com

Limitation of Liability

Measurement Computing cannot be held liable for any damages resulting from the use or misuse of this product.

Copyright, Trademark, and Licensing Notice

All Measurement Computing documentation, software, and hardware are copyright with all rights reserved. No part of this product may be copied, reproduced or transmitted by any mechanical, photographic, electronic, or other method without Measurement Computing's prior written consent. IOtech product names are trademarked; other product names, as applicable, are trademarks of their respective holders. All supplied IOtech software (including miscellaneous support files, drivers, and sample programs) may only be used on one installation. You may make archival backup copies.

CE Notice



Many Measurement Computing products carry the CE marker indicating they comply with the safety and emissions standards of the European Community. When applicable these products have a Declaration of Conformity stating which specifications and operating conditions apply. You can view the Declarations of Conformity at www.mccdaq.com/legal.aspx (CE Information page).

Warnings, Cautions, Notes, and Tips



Refer all service to qualified personnel. This caution symbol warns of possible personal injury or equipment damage under noted conditions. Follow all safety standards of professional practice and the recommendations in this manual. Using this equipment in ways other than described in this manual can present serious safety hazards or cause equipment damage.



This warning symbol is used in this manual or on the equipment to warn of possible injury or death from electrical shock under noted conditions.



This ESD caution symbol urges proper handling of equipment or components sensitive to damage from electrostatic discharge. Proper handling guidelines include the use of grounded anti-static mats and wrist straps, ESD-protective bags and cartons, and related procedures.



This symbol indicates the message is important, but is not of a Warning or Caution category. These notes can be of great benefit to the user, and should be read.



In this manual, the book symbol always precedes the words "Reference Note." This type of note identifies the location of additional information that may prove helpful. References may be made to other chapters or other documentation.



Tips provide advice that may save time during a procedure, or help to clarify an issue. Tips may include additional reference.

Specifications and Calibration

Specifications are subject to change without notice. Significant changes will be addressed in an addendum or revision to the manual. As applicable, the hardware is calibrated to published specifications. Periodic hardware calibration is not covered under the warranty and must be performed by qualified personnel as specified in this manual. Improper calibration procedures may void the warranty.

Your order was carefully inspected prior to shipment. When you receive your system, carefully unpack all items from the shipping carton and check for physical signs of damage that may have occurred during shipment. Promptly report any damage to the shipping agent and your sales representative. Retain all shipping materials in case the unit needs returned to the factory.

CAUTION



Using this equipment in ways other than described in this manual can cause personal injury or equipment damage. Before setting up and using your equipment, you should read *all* documentation that covers your system. Pay special attention to Warnings and Cautions.

Note: During software installation, Adobe® PDF versions of user manuals will automatically install onto your hard drive as a part of product support. The default location is in the **Programs** group, which can be accessed from the *Windows Desktop*. Initial navigation is as follows:

Start [Desktop “Start” pull-down menu]
⇒ **Programs**
⇒ **IOtech DaqX Software**

You can also access the PDF documents directly from the data acquisition CD by using the <**View PDFs**> button located on the opening screen.

Refer to the PDF documentation for details regarding both hardware and software.

A copy of the Adobe Acrobat Reader® is included on your CD. The Reader provides a means of reading and printing the PDF documents. Note that hardcopy versions of the manuals can be ordered from the factory.

Table of Contents

Personal Daq/3000 Series, Installation Guide (p/n 1136-0940)

1 – Device Overviews

- Block Diagrams 1-1*
- Connections 1-2*
- Theory of Operation..... 1-3*
- Software 1-15*

2 – Connections and Pinouts

- Overview 2-1*
- Pinout for Personal Daq/3000 Series Modules 2-2*
- PDQ30 Analog Expansion Option 2-3*
- Connecting for Single-Ended or Differential 2-5*

3 – CE-Compliance

- Overview 3-1*
- CE Standards and Directives 3-1*
- Safety Conditions 3-2*
- Emissions/Immunity Conditions 3-2*

4 – Calibration

5 – Counter Input Modes

- Tips for Making High-Speed Counter Measurements (> 1 MHz) 5-1*
- Debounce Module 5-1*
- Terms Applicable to Counter Modes.....5-5*
- Counter Options 5-5*
- Counter/Totalize Mode 5-6*
- Period Mode 5-8*
- Pulsewidth Mode 5-11*
- Timing Mode 5-13*
- Encoder Mode 5-15*

6 – Setpoint Configuration for Output Control

Overview 6-1

Detecting Input Values 6-3

Controlling Analog, Digital, and Timer Outputs 6-4

P2C, DAC, or Timer Update Latency 6-6

More Examples of Control Outputs 6-7

Detection on an Analog Input, DAC and P2C Updates 6-7

Detection on an Analog Input, Timer Output Updates 6-8

Using the Hysteresis Function 6-8

Using Multiple Inputs to Control One DAC Output 6-10

The Setpoint Status Register 6-11

7 – Specifications – Personal Daq/3000 Series and PDQ30

Appendix A: Signal Modes and System Noise

Signal Modes A-1

Connecting Thermocouples to Screw-Terminal Blocks A-2

Shielding A-3

TC Common Mode A-3

Cold Junction Compensation Techniques A-4

System Noise A-5

Averaging A-5

Analog Filtering A-5

Input and Source Impedance A-5

Crosstalk A-5

Oversampling and Line Cycle Rejection A-6

Glossary

USB1-MHz, 16-Bit Multifunction Modules



Before you get started

Verify that you have the following items.

- Personal Daq/3000 Series Device(s)
- Data Acquisition CD
- Monitor: SVGA, 1024 x 768 screen resolution
- Computer that meets or exceeds the following:
Intel™ Pentium, 1 GHz or equivalent; 10 GB disk space;
Available USB Port; USB cable; one of the following
Microsoft® Operating Systems and indicated memory or
higher:
WindowsXP – 128 MB memory
Windows2000 – 128 MB memory
Windows Vista – 1 GB memory

Step 1 – Install Software

IMPORTANT: Software must be installed before installing hardware.

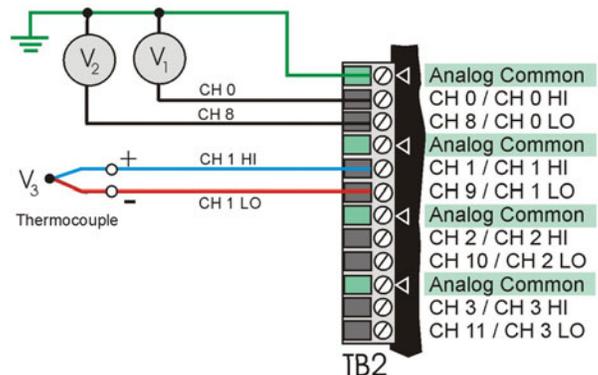
1. Place the Data Acquisition CD into the CD-ROM drive. *Wait for PC to auto-run the CD. This may take a few moments, depending on your PC.* If the CD does not auto-run, use the Desktop's Start/Run/Browse feature and run the **Setup.exe**.
2. After the intro-screen appears, follow the screen prompts.

Step 2 – Connect Signal Lines and Hardware

1. Connect signal lines to the removable screw-terminal blocks.

Voltage signals can be connected using the *Single-Ended* method. In the figure, voltage source V1 is connected to Channel 0 and to analog common; and voltage source V2 is connected to Channel 8 and the same analog common connection.

The figure shows voltage V3 resulting from a thermocouple. In this case *Differential* mode is being used. The HI (+) line from the thermocouple is shown connected to Channel 1 HI; and the LO (negative) side is connected to Channel 1 LO. Notice that Channel 1 LO is the same screw terminal connection that would be used for CH 9 Single-Ended.



To differentially connect a thermocouple; connect the red T/C wire to the channel's Low (L) connector. Connect the *other color* wire to the channel's High (H) connector.

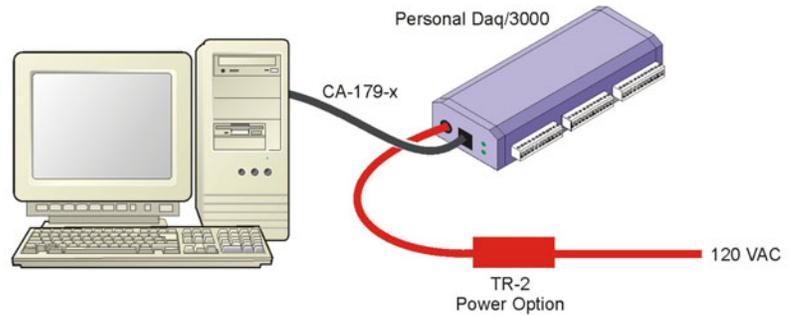
PDQ30 is an optional analog expansion module that can be used to add an additional 48 SE (or 24 DE) analog inputs. **PDQ30 is not to be connected to a live device. Unplug the USB cable from the host PC prior to connecting the PDQ30.** Refer to user's manual for regarding PDQ30 issues.

Power Consumption (Typical) ¹			
Model	Consumption ²	TR-2 ²	Notes
/3000	2500 mW	Recommended	¹ The power consumption listed is for a single /3000 Series device, or for a single device connected to a PDQ30 expansion module. ² A power adapter (TR-2) will be required if the USB port cannot supply adequate power. When meeting USB2 standards, a USB port can supply 2500 mW (nominal at 5V, 500 mA).
/3001	3000 mW	Required	
/3005	2000 mW	Optional	
/3000 & PDQ30	2900 mW	Required	
/3001 & PDQ30	3400 mW	Required	
/3005 & PDQ30	2400 mW	Recommended	



If using a TR-2, be sure to supply power from it to the Personal Daq/3000 *before connecting the USB cable to the computer*. This allows the device to inform the host computer [upon connection of the USB cable] that the unit requires minimal power from the computer's USB port.

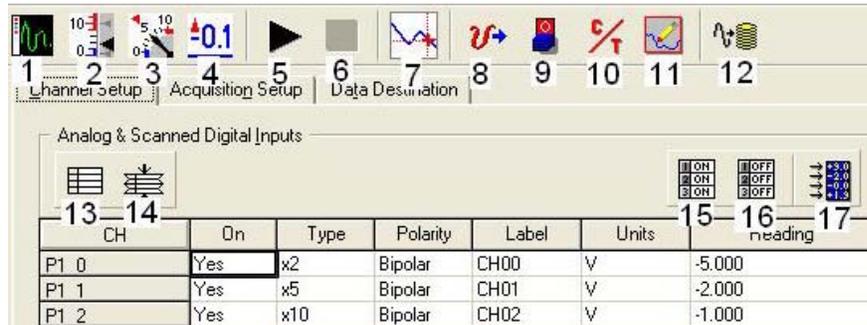
Use a CA-179-x USB cable to connect the Personal Daq/3000 Series device to a USB port on the computer. Note that use of a PC with a USB2.0 port is recommended. A USB1.1 port will work, but will result in lower performance.



Step 3 - Start DaqView & Configure the System

From Windows, open DaqView by double clicking on its icon, or use the Windows Desktop Start menu to access the program. You will find *DaqView* listed in the Program group (Use the desktop Start Menu / Programs to access the group).

Once the program is executed, software automatically identifies your Personal Daq/3000 Series device and brings up DaqView's *Main Window*.



Button Reference

(1) Scope	(2) Bar Graph Meters	(3) Analog Meters	(4) Digital Meters	(5) Start All Indicators	(6) Stop All Indicators
(7) View File Data	(8) Analog Output	(9) Digital I/O	(10) Counter/Timer	(11) Waveform & Pattern Output	(12) Acquire
(13) Show ALL Channels	(14) Hide INACTIVE Channels	(15) Turn All Visible Channels ON	(16) Turn All Channels OFF	(17) Channel Reading	

To configure channels, make the desired changes in the *Channel Setup* window. This window displays the analog and scanned digital input channels and allows you to configure; for example: you can change a channel from bipolar to unipolar and can change its units.

To configure acquisition parameters, select the second tab (below numbers 4 & 5 in the above figure). This displays the *Acquisition Setup* window, which you can use to set triggering and configure the scan. The settings will be used when an acquisition is started.

To assign a filename and folder, select the third tab (below numbers 6 & 7 in the above figure). This displays the *Data Destination* window, which provides a means of designating the desired file names, file formats, and the directory for saving the acquired data.

To collect data, Click the <Enable Readings Column> button (17), or the <Start All Indicators button> (5); the data acquisition begins and the *readings* column becomes active. Click the <Acquire> button (12) to send the data to disk.

Click one of the toolbar's display icon buttons to see your data in the form of a scope or meter display. Click the <Scope> button (1) to bring up the *Scope window*. This allows you to set up scope and chart displays. Buttons 2, 3, and 4 are for bar graph meters, analog meters, and digital meters. Note that you can simultaneously view combinations of display types.

Note: For detailed information, view the PDF documentation located on CD, at our website, or in the Programs Group [which resides on your PC, after software installation].



324400D-01

- Block Diagrams 1-1
- Connections 1-2
- Product Features 1-3
- Software 1-15

 **DaqView can only be used with one Personal Daq at a time. DASyLab and LabView can be used with multiple modules. For multiple module use (via custom programming) refer to the *Using Multiple Devices* section of the *Programmer's Manual*.**



Reference Note:

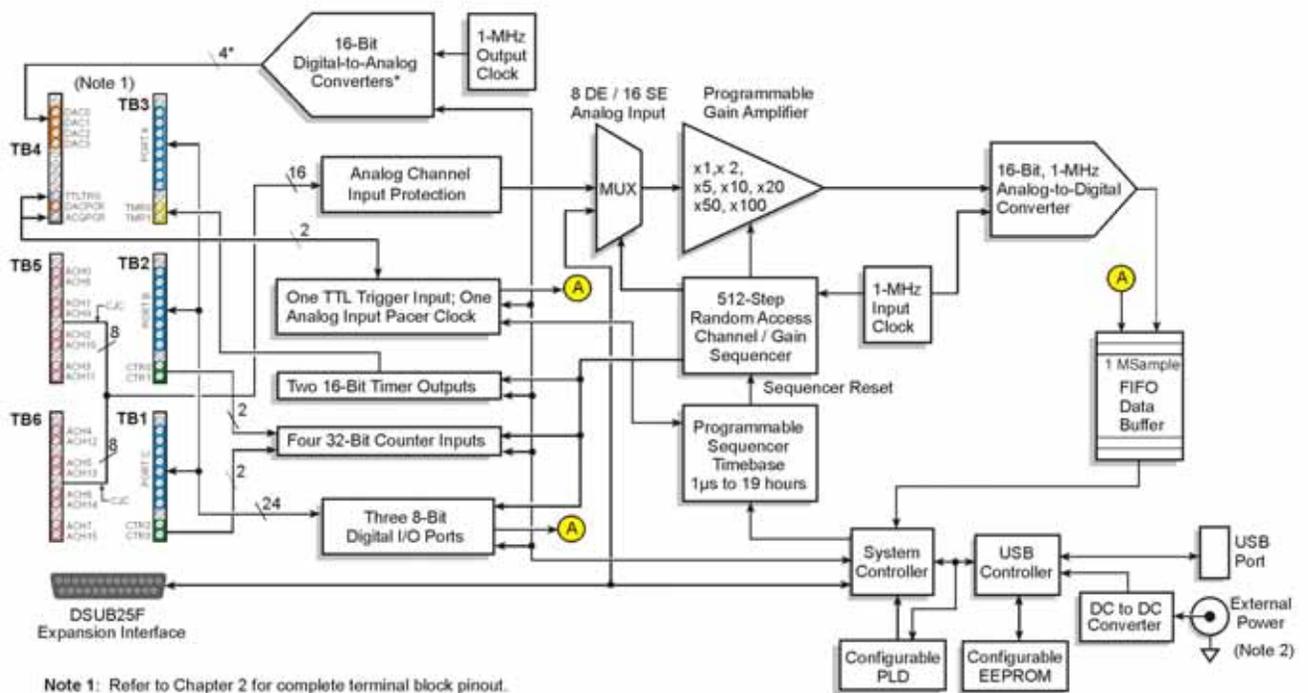
Programming topics are covered in the *Programmer's User Manual* (p/n 1008-0901). As a part of product support, this manual is automatically loaded onto your hard drive during software installation. The default location is the Programs group, which can be accessed through the Windows Desktop.



Reference Note:

For module details refer to Chapter 7, *Specifications*.

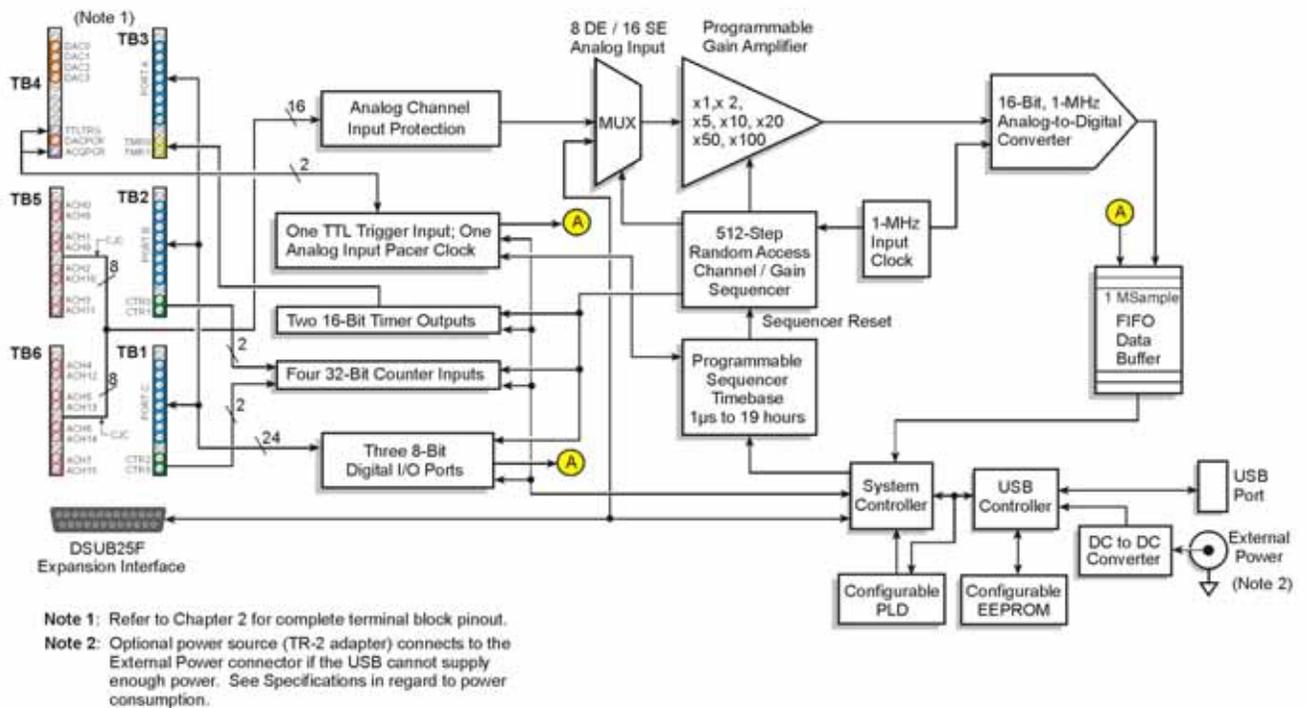
Block Diagrams



Note 1: Refer to Chapter 2 for complete terminal block pinout.
Note 2: Optional power source (TR-2 adapter) connects to the External Power connector if the USB cannot supply enough power. See Specifications in regard to power consumption.

Block Diagram for Personal Daq/3000 and /3001

*Personal Daq/3000 has two 16-Bit Digital-to-Analog Converters. Personal Daq/3001 has four 16-Bit Digital-to-Analog Converters.



Block Diagram for Personal Daq/3005

Connections



Reference Note:

For the Personal Daq/3000 Series **installation procedure**, refer to the *Personal Daq Installation Guide (1136-0940)*. A copy of the guide is included at the beginning of this manual.

- USB2.0*** Used to connect the Personal Daq/3000 Series device to a host PC [or USB hub] via one of the following cables: CA-179-1, CA-179-3, CA-179-5 (1 m, 3m, and 5m lengths, respectively)
- External Power** Used to connect the device to an optional TR-2 external power supply when the host PC's USB connector cannot supply enough power or when an independent source of power is desired.
- DSUB25F** The 25-pin (female) connector can connect directly to a PDQ30, or can connect to a PDQ30 indirectly via a CA-96A cable.
- Screw Terminal Blocks** Six removable screw-terminal blocks provide connection for signal I/O. Each device in the series supports 16SE/8DE Analog Inputs, 24 Digital I/O, 4 Counters, and 2 Timers. In addition, the /3000 model supports 2 Analog Outputs; and the /3001 model supports 4 Analog Outputs. Connections are labeled on the devices. Pinouts are included in Chapter 2.

* Use with USB1.1 will result in lower transfer speed which may not support continuous data collection at high scan rates.

Product Features

I/O Comparison Matrix						
Product or System	Analog Input Channels 	Input Ranges	Analog Output Channels 	Digital I/O Channels 	Counter Inputs 	Timer Outputs 
Personal Daq/3000	16SE / 8DE	7	2	24	4	2
Personal Daq/3001	16SE / 8DE	7	4	24	4	2
Personal Daq/3005	16SE / 8DE	7	0	24	4	2
Personal Daq/3000 with PDQ30	64SE / 32DE	7	2	24	4	2
Personal Daq/3001 with PDQ30	64SE / 32DE	7	4	24	4	2
Personal Daq/3005 with PDQ30	64SE / 32DE	7	0	24	4	2

The Personal Daq/3000 Series modules feature a 16-bit/1-MHz A/D converter, 16 analog input channels [user expandable up to 64], up to four 16-bit/1-MHz analog outputs, 24 high-speed digital I/O channels, 2 timer outputs, and four 32-bit counters.

All analog I/O, digital I/O, and counter/timer I/O can operate synchronously and simultaneously, guaranteeing deterministic I/O timing amongst all signal types. The Personal Daq/3000 Series modules include a high-speed, low-latency, highly deterministic control output mode that operates independent of the PC. In this mode both digital and analog outputs can respond to analog, digital and counter inputs as fast as 2 μ sec.

Other Hardware Features Include:

- Encoder measurements up to 20 MHz, including Z-channel zeroing
- Frequency and Pulse-width measurements with 20.83 nsec resolution
- Timing mode: can measure the time between two counter inputs to 20.83 nsec resolution
- Self-calibration

The Personal Daq/3000 series offers up to 4-MHz scanning of all digital input lines. Digital inputs and counter inputs can be synchronously scanned [along with analog inputs] but do not affect the overall A/D rate because they use no time slot in the scanning sequencer. For example, one analog input can be scanned at the full 1-MHz A/D rate along with digital and counter input channels. The 1-MHz A/D rate is unaffected by additional digital and counter channels.

Adding analog input channels to a Personal Daq/3000 Series module is easy. An additional 48 single-ended [or 24 differential] analog input channels can be added to each module with the optional PDQ30 expansion module. The PDQ30 connects to the Personal Daq/3000 series card via an external cable. With the Personal Daq/3000's 1-MHz aggregate sample rate, users can easily add multiple analog expansion channels and still have enough bandwidth to have a per-channel sample rate in the multiple kHz range.

Although the Personal Daq/3000 Series modules are powered via a USB port on a host PC, an external power connector is available for cases in which the host PC's USB port cannot supply adequate power, or for when the user prefers a separate power source. The TR-2 is an optional power supply available for this purpose. The TR-2 plugs into a standard 120VAC outlet and will supply 9VDC, 1 amp power to the module via its external power connector.

Signal I/O

Six banks of removable screw-terminal blocks provide connectivity to the 16SE/8DE analog input channels, 24 digital I/O lines, counter/timer channels, and analog outputs (when applicable).

Analog Input

The Personal Daq/3000 series has a 16-bit, 1-MHz A/D coupled with 16 single-ended, or 8 differential analog inputs. Seven software programmable ranges provide inputs from $\pm 10\text{V}$ to $\pm 100\text{ mV}$ full scale. Each channel can be software-configured for a different range, as well as for single-ended or differential bipolar input. Each differential channel can accept any type of thermocouple input.

Synchronous I/O

The Personal Daq/3000 series has the ability to make analog measurements and scan digital and counter inputs, while synchronously generating up to four analog outputs.

Additionally, while digital inputs and counter inputs can be synchronously scanned along with analog inputs, they do not affect the overall A/D rate because they use no time slot in the scanning sequencer. For example, one analog input can be scanned at the full 1-MHz A/D rate along with digital and counter input channels. The 1-MHz A/D rate is unaffected by the additional digital and counter channels.

Input Scanning

Personal Daq/3000 Series devices have several scanning modes to address a wide variety of applications. A 512-location scan buffer can be loaded by the user with any combination of analog input channels. All analog input channels in the scan buffer are measured sequentially at 1 μsec per channel. The user can also specify that the sequence repeat immediately, or repeat after a programmable delay from 0 to 19 hours, with 20.83 nsec resolution. For example, in the fastest mode, with a 0 delay, a single analog channel can be scanned continuously at 1 Msamples/s; two analog channels can be scanned at 500K samples/each; 16 analog input channels can be scanned at 62.5 Ksamples/s.

The digital and counter inputs can be read in several modes. First, via software the digital inputs or counter inputs can be read *asynchronously* at anytime before, during, or after an analog input scan sequence. This software mode is not deterministic as to exactly when a digital or counter input is read relative to an analog input channel.

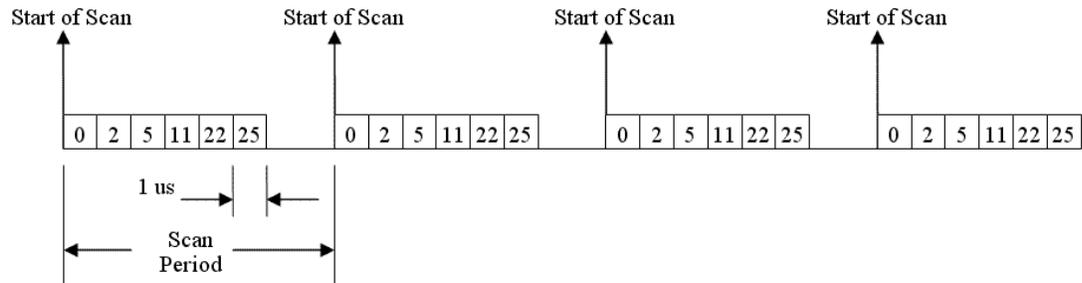
In either of the two synchronous modes, the digital inputs and/or counter inputs are read with deterministic time correlation to the analog inputs. In the *once-per-scan mode*, all of the enabled digital inputs and counter inputs are read during the first analog measurement of an analog input scan sequence. The advantage of this mode is that the digital and counter inputs do not consume an analog input time slot, and therefore do not reduce the available bandwidth for making analog input measurements. For example, presume all 24 bits of digital input are enabled, and all four 32-bit counters are enabled, and eight channels of analog inputs are in the scan sequence at full 1 $\mu\text{sec}/\text{channel}$ rate. At the beginning of each analog input scan sequence, which would be 8 μsec in total duration, all digital inputs and counter inputs will be measured and sent to the PC during the first μsec of the analog scan sequence.

Another synchronous mode allows digital inputs to be scanned every time an analog input channel is scanned. For example, if eight analog inputs are scanned at 1 μsec per channel continuously, and 24 bits of digital inputs are enabled, then the 24 bits of digital inputs will be scanned at 24 bits per 1 μsec . If counters are enabled in this mode, they will be scanned at once per scan, in the same manner as in the first example above.

Note: It is not necessary to read counters as often as it is to read digital inputs. This is because counters continue to count pulses regardless of whether or not they are being read by the PC.

Example 1: Analog channel scanning of voltage inputs

The figure below shows a simple acquisition. The scan is programmed pre-acquisition and is made up of 6 analog channels (Ch0, Ch2, Ch5, Ch11, Ch22, Ch25.) Each of these analog channels can have a different gain. The acquisition is triggered and the samples stream to the PC via USB2. Each analog channel requires one microsecond of scan time therefore the scan period can be no shorter than 6 us for this example. The scan period can be made much longer than 6 us, up to 19 hours. The maximum scan frequency is one divided by 6us or 166,666 Hz.

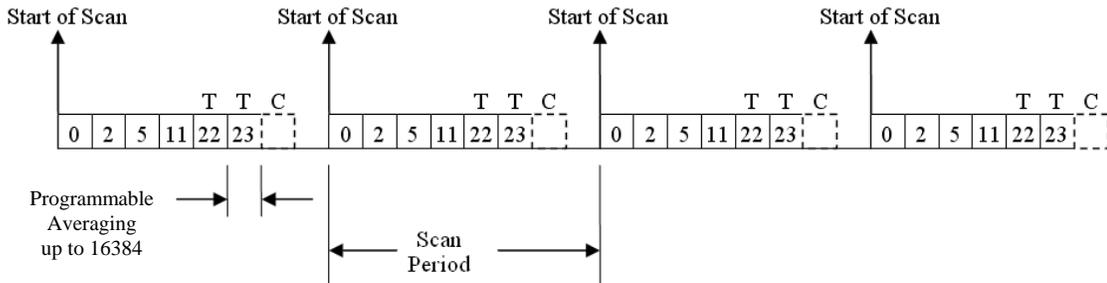


Notice that some of the analog channels in the scan group are from a PDQ30 expansion module. All analog channels are sampled at the same rate of 1us. Analog channels on the PDQ30 can also have any of the gain ranges applied.

Example 2: Analog channel scanning of voltage and temperature inputs

The figure below shows a more complicated acquisition. The scan is programmed pre-acquisition and is made up of 6 analog channels (Ch0, Ch2, Ch5, Ch11, Ch22, Ch23.) Each of these analog channels can have a different gain. Two of the channels (22 and 23) are from a PDQ30 expansion module. These two channels can be programmed to directly measure thermocouples. In this mode, oversampling is programmable up to 16384 oversamples per channel in the scan group. When oversampling is applied, it is applied to all analog channels in the scan group, including temperature and voltage channels. (Digital channels are not oversampled.) If the desired number of oversamples is 256 then each analog channel in the scan group will take 256 microseconds, the returned 16-bit value represents an average of 256 consecutive 1us samples of that channel. The acquisition is triggered and 16-bit values (each representing an average of 256) stream to the PC via USB2.

Since two of the channels in the scan group are temperature channels, the acquisition engine will be required to read a cold-junction-compensation (CJC) temperature every scan. In fact, depending upon which PDQ30 channels are being used for temperature, there may be a CJC temperature required for each temperature channel in the scan. Each 4 channel terminal block of the PDQ30 shares one CJC so if all temperature channels are grouped on one (of the six) terminal blocks, then only one CJC temperature measurement will need to be made per scan. For every PDQ30 terminal block that is measuring at least one temperature channel, one additional CJC temperature measurement will be automatically added to the scan group. This increases the scan period and reduces the maximum scanning frequency.



In this example, the desired number of oversamples is 256, therefore each analog channel in the scan group requires 256 microseconds to return one 16-bit value. The oversampling is also done for CJC temperature measurement channels. The minimum scan period for this example is therefore $7 \times 256 \mu\text{s}$, or 1792 microseconds. The maximum scan frequency is the inverse of this number, 558 Hz.

Channels 0 through 7 of the Personal Daq/3000 can be used to measure temperature in place of voltage. There are three CJC channels per analog input terminal block. When all 8 differential analog inputs are used for temperature 6 CJC channels must be included as part of the scan group. This means when the device is measuring all 8 temperature inputs and using oversampling of 256, the minimum scan period is $14 \times 256 \mu\text{s}$, or 3584 μs .

Autozero may also be employed. This adds more channels to the scan group and further reduces the maximum scan frequency. Auto zero channels read a shorted analog input that is internal to the PDQ30 or PersonalDaq/3000 Series module. Auto zeroing reduces drift due to fluctuating ambient temperatures or ambient temperatures outside the DC specifications.

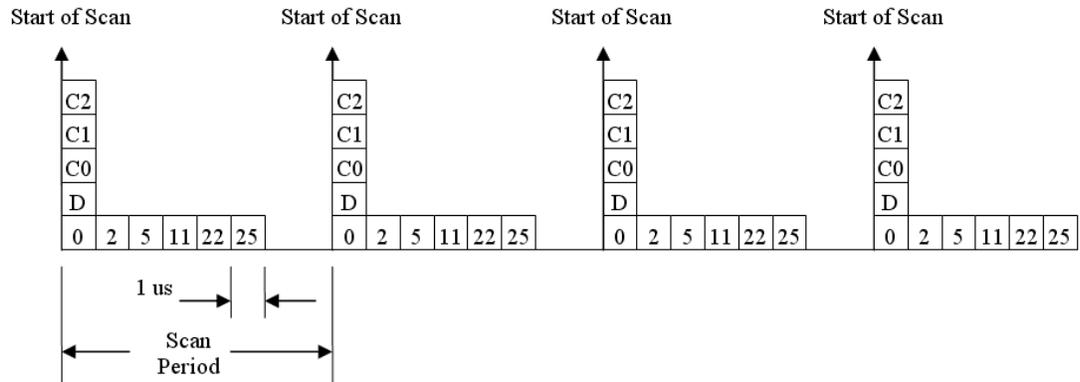


Reference Note:

Appendix A includes detailed information regarding signal modes, methods of noise reduction, and averaging techniques.

Example 3: Analog and digital channel scanning, once per scan mode

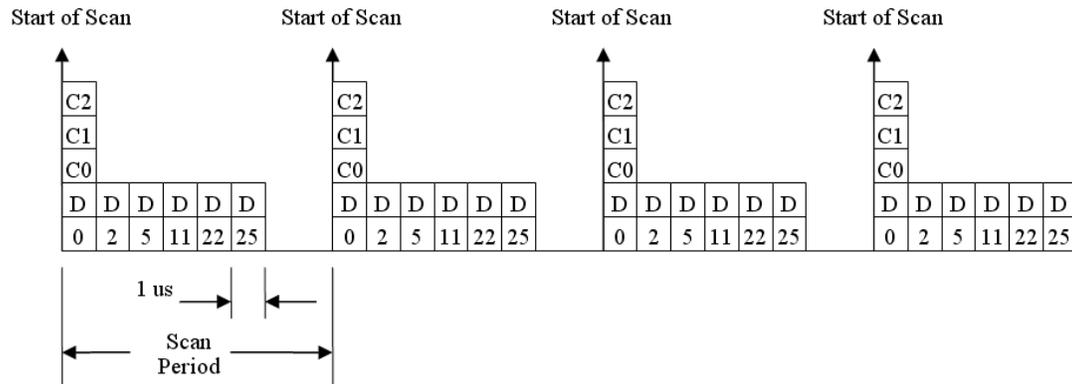
The figure below shows a more complicated acquisition. The scan is programmed pre-acquisition and is made up of 6 analog channels (Ch0, Ch2, Ch5, Ch11, Ch22, Ch25) and 4 digital channels (16-bits of digital IO, 3 counter inputs.) Each of the analog channels can have a different gain and each of the counter channels can be put into a different mode (totalizing, pulsewidth, encoder, etc.) The acquisition is triggered and the samples stream to the PC via USB2. Each analog channel requires one microsecond of scan time therefore the scan period can be no shorter than 6 us for this example. All of the digital channels are sampled at the start of scan and do not require additional scanning bandwidth as long as there is at least one analog channel in the scan group. The scan period can be made much longer than 6 us, up to 19 hours. The maximum scan frequency is one divided by 6us or 166,666 Hz.



The counter channels could be returning only the lower 16-bits of count value if that is sufficient for the application. They could also be returning the full 32-bit result if necessary. Similarly, the digital input channel could be the full 24 bits if desired or only 8 bits if that is sufficient. If the 3 counter channels are all returning 32 bit values and the digital input channel is returning a 16 bit value, then 13 samples are being returned to the PC every scan period, each sample being 16-bits. 32-bit counter channels are divided into two 16-bit samples, one for the low word and the other for the high word. If the maximum scan frequency is 166,666 Hz then the data bandwidth streaming into the PC is 2.167 MSamples per second. Some slower PCs may have a problem with data bandwidths greater than 6 MSamples per second. All Personal Daq/3000 Series devices have an onboard 1 Msample buffer for acquired data.

Example 4: Sampling digital inputs for every analog sample in a scan group

The figure below shows another acquisition. The scan is programmed pre-acquisition and is made up of 6 analog channels (Ch0, Ch2, Ch5, Ch11, Ch22, Ch25) and 4 digital channels (16-bits of digital input, 3 counter inputs.) Each of the analog channels can have a different gain and each of the counter channels can be put into a different mode (totalizing, pulsewidth, encoder, etc.) The acquisition is triggered and the samples stream to the PC via USB2. Each analog channel requires one microsecond of scan time therefore the scan period can be no shorter than 6 us for this example. All of the digital channels are sampled at the start of scan and do not require additional scanning bandwidth as long as there is at least one analog channel in the scan group. The 16-bits of digital input are sampled for every analog sample in the scan group. This allows up to 1MHz digital input sampling while the 1MHz analog sampling bandwidth is aggregated across many analog input channels. The scan period can be made much longer than 6 us, up to 19 hours. The maximum scan frequency is one divided by 6us or 166,666 Hz. Note that digital input channel sampling is not done during the “dead time” of the scan period where no analog sampling is being done either.



If the 3 counter channels are all returning 32 bit values and the digital input channel is returning a 16 bit value, then 18 samples are being returned to the PC every scan period, each sample being 16-bits. 32-bit counter channels are divided into two 16-bit samples, one for the low word and the other for the high word. If the maximum scan frequency is 166,666 Hz then the data bandwidth streaming into the PC is 3 MSamples per second. Some slower PCs may have a problem with data bandwidths greater than 6 MSamples per second. All Personal Daq/3000 Series devices have an onboard 1 Msample buffer for acquired data.

Analog Input & Channel Expansion

The Personal Daq/3000 series has a 16-bit, 1-MHz A/D coupled with 16 single-ended, or 8 differential analog inputs. Seven software programmable ranges provide inputs from $\pm 10V$ to ± 100 mV full scale. Each channel can be software-configured for a different range, as well as for single-ended or differential bipolar input.

Adding additional analog input channels to the /3000 series modules is easy with the optional PDQ30 expansion module. The PDQ30 can connect directly to the Personal Daq's female DSUB25 connector, or be connected via cable (CA-96A). PDQ30 adds an additional 48 single-ended or [24 differential-ended] analog inputs for a total channel capacity of 64 single-ended [or 32 differential] inputs.

Measurement speed of PDQ30 channels is the same 1 Msample/s exhibited by the /3000 module channels.

USB2.0 versus USB1.1

Connecting a Personal Daq/3000 Series device to a USB1.1 port or hub will result in lower transfer speed which may not support continuous data collection at high scan rates. Note that *Hi-Speed* (USB2.0) ports are forty times faster than the earlier *Full-Speed* (USB1.1) versions.

When a computer has a board with USB 2.0 ports, an “Enhanced” USB controller can be found in the Device Manager. The Device Manager will also show two other USB controllers. This is due to the fact that USB2.0 circuitry includes 3 chips [one for the actual USB2.0 capable devices and two for backward USB1.1 compatibility]. Thus a USB 2.0 motherboard can host any USB device (version 2.0 or lower), assuming there are no defects with the board, system, and/or device.

Notes on USB Hubs:

- USB 1.1 (obsolete) hubs will work on USB 2.0 ports, but cannot utilize USB 2.0 capabilities.
- Hi-Speed and Full/Low-Speed USB devices can coexist on USB 2.0 hubs.
- USB 2.0 hubs can be used on computers with USB 1.1 ports, but will not exhibit USB 2.0 capabilities.
- Minimize hub use and keep USB cables as short as possible.
- Regardless of the USB hub or port used, if power to the Personal Daq/3000 Series device is insufficient, connect a TR-2 power adapter to the unit's External Power jack.
- Only self-powered hubs can supply sufficient power (500 mA at 5V nominal). Verify that the AC-to-DC power supply for the self-powered hub can supply at least 2.1 amps at 5 volts.
- In general, do not use more than three Personal Daq/3000 systems per one self-powered hub.

Triggering

Triggering can be the most critical aspect of a data acquisition application. The Personal Daq/3000 series supports a full complement of trigger modes to accommodate any measurement situation.

Hardware Analog Triggering. The Personal Daq/3000 Series uses true analog triggering, whereby the trigger level programmed by the user sets an analog DAC, which is then compared in hardware to the analog input level on the selected channel. The result is analog trigger latency which is guaranteed to be less than 1.3 μ s. Any analog channel can be selected as the trigger channel, including built-in or PDQ30 expansion channels. The user can program the trigger level, as well as the rising or falling edge, and hysteresis.



When the starting out analog input voltage is near the trigger level, and you are performing a rising [or falling] hardware analog level trigger, it is possible that the analog level comparator will have already tripped, i.e., to have tripped before the sweep was enabled.

If this is the case, the circuit will wait for the comparator to change state. However, since the comparator has already changed state, the circuit will not see the transition.

- Solution:**
- (1) Set the analog level trigger to the desired threshold.
 - (2) Apply an analog input signal that is *more than 2.5%* of the full-scale range *away from the desired threshold*. This ensures that the comparator is in the proper state at the beginning of the acquisition.
 - (3) Bring the analog input signal toward the desired threshold. When the input signal is at the threshold (\pm some tolerance) the sweep will be triggered.
 - (4) Before re-arming the trigger, again move the analog input signal to a level that is more than 2.5% of the full-scale range *away from* the desired threshold.

- Example:**
- an engineer is using the ± 2 V full-scale range (gain = 5)
 - he desires to trigger at +1V on the rising edge
 - he sets the analog input voltage to an initial start-value which is *less than* +0.9V ($1\text{V} - (2\text{V} * 2 * 2.5\%)$).

Digital Triggering. A separate digital trigger input line is provided, allowing TTL-level triggering with latencies guaranteed to be less than 1 μ s. Both the logic levels (1 or 0), as well as the rising or falling edge can be programmed for the discrete digital trigger input.

Pattern Triggering. The user can specify a 16-bit digital pattern to trigger an acquisition, including the ability to mask or ignore specific bits.

Software-Based Channel Level Triggering. This mode differs from the modes just discussed because the readings [analog, digital, or counter] are interrogated by the PC in order to detect the trigger event. Triggering can also be programmed to occur when one of the counters reaches, exceeds, or is within a programmed window.

Any of the built-in counter/totalizer channels can be programmed as a trigger source. Triggers can be detected on scanned digital input channel patterns as well. Normally software-based triggering results in long latencies from the moment a trigger condition is detected until the instant data is acquired. However, the Personal Daq/3000 Series circumvents this undesirable situation by use of pre-trigger data. Specifically, when software-based-triggering is employed, and the PC detects that a trigger condition has occurred, (which may be thousands of readings after the actual occurrence of the signal), the Personal Daq driver automatically looks back to the location in memory, to where the actual trigger-causing measurement occurred. The acquired data presented to the user begins at the point where the trigger-causing measurement occurs. The maximum latency in this mode is equal to one scan period

Stop Trigger. Any of the software trigger modes previously described, including scan count, can be used to stop an acquisition. Thus an acquisition can be programmed to begin on one event, such as a voltage level, and then can stop on another event, such as a digital pattern.

Pre-Triggering and Post-Triggering Modes. Six modes of pre-triggering and post-triggering are supported, providing a wide variety of options to accommodate any measurement requirement. When using pre-trigger, the user must use software-based triggering to initiate an acquisition. The six modes are:

- ***No pre-trigger, post-trigger stop event.*** This, the simplest of modes, acquires data upon receipt of the trigger, and stops acquiring upon receipt of the stop-trigger event.
- ***Fixed pre-trigger with post-trigger stop event.*** In this mode, the user specifies the number of pre-trigger readings to be acquired, after which, acquisition continues until a stop-trigger event occurs.
- ***No pre-trigger, infinite post-trigger.*** No pre-trigger data is acquired in this mode. Instead, data is acquired beginning with the trigger event, and is terminated when the operator issues a command to halt the acquisition.
- ***Fixed pre-trigger with infinite post-trigger.*** The user specifies the amount of pre-trigger data to acquire, after which the system continues to acquire data until the program issues a command to halt acquisition.
- ***Variable pre-trigger with post trigger stop event.*** Unlike the previous pre-trigger modes, this mode does not have to satisfy the pre-trigger number of readings before recognizing the trigger event. Thus the number of pre-trigger readings acquired is variable and dependent on the time of the trigger event relative to the start. In this mode, data continues to be acquired until the stop trigger event is detected. *Driver support only.*
- ***Variable pre-trigger with infinite post trigger.*** This is similar to the mode described above, except that the acquisition is terminated upon receipt of a command from the program to halt the acquisition. *Driver support only.*

Calibration

Every range of a Personal Daq/3000 Series device is calibrated at the factory using a digital NIST traceable calibration method. This method works by storing a correction factor for each range on the unit at the time of calibration. The user can adjust the calibration of the board while it is installed in the acquisition system without destroying the factory calibration. This is accomplished by having 3 distinct calibration tables in the on-board EPROM.

The user can select any of the three cal tables provided [factory, user, or self-cal tables] by API call or from within software. Self-cal can be performed automatically via the included software and without the use of external hardware or instruments. Self-cal derives its traceability through an on-board reference which has a stability of 0.005% per year.

Note that a 2-year calibration period is recommended for Personal Daq/3000 Series modules.



Reference Note:

Chapter 4, *Calibration*, discusses using a temperature calibrator with a Personal Daq/3000 Series module.

Analog Output

Personal Daq/3000 and /3001 Only

Personal Daq/3000 has two 16-bit, 1 MHz analog output channels. Personal Daq/3001 has four such channels. Analog outputs can be updated at a maximum rate of 1 MHz.

The channels have an output range of -10V to +10V. Each D/A can continuously output a waveform. This can be read from PC RAM or from a file on the hard disk. In addition, a program can asynchronously output a value to any of the D/As for non-waveform applications, presuming that the D/A is not already being used in the waveform output mode.

When used to generate waveforms, the D/As can be clocked in several different modes. Each D/A can be separately selected to be clocked from one of the following sources.

- **Asynchronous Internal Clock**. The internal programmable clock can generate updates ranging from 1.5 Hz to 19 hours, independent of any acquisition rate.
- **Synchronous Internal Clock**. The rate of analog output update can be synchronized to the acquisition rate derived from 1 MHz to once every 19 hours.
- **Asynchronous External Clock**. A user-supplied external input clock can be used to pace the D/A, entirely independent of analog inputs.
- **Synchronous External Clock**. A user-supplied external input clock can pace both the D/A and the analog input.

Digital Inputs and Outputs

Twenty-four TTL-level digital I/O lines are included in each of the Personal Daq/3000 Series modules. Digital I/O can be programmed in 8-bit groups as either inputs or outputs and can be scanned in several modes (see *Input Scanning*). Ports programmed as input can be part of the scan group and *scanned along with analog input channels*, or can be asynchronously accessed via the PC at any time, including when a scanned acquisition is occurring.

Two synchronous modes are supported when digital inputs are scanned along with analog inputs.

- **Scanning digital inputs at the start of each scan sequence.** In this mode the digital inputs are scanned at the start of each scan sequence, which means the rate at which they are scanned is dependent on the number of analog input channels and the delay period. For example, if 8 analog inputs were enabled with a 0 delay period, then the digital inputs in this mode would be scanned at once per 8 μ sec, i.e., 125 kHz.
- **Scanning digital inputs synchronously with every analog input channel.** In this synchronous mode, the enabled digital inputs are scanned synchronously with every analog input channel. So in the preceding example the digital inputs would be scanned at once per μ sec, or 1 MHz. If no analog inputs were being scanned the digital inputs could be scanned at up to 4 MHz.

Digital Outputs and Pattern Generation

Digital outputs can be updated asynchronously at anytime before, during or after an acquisition. Two of the 8-bit ports can also be used to generate a 16-bit digital pattern at up to 4 MHz. The Personal Daq/3000 Series modules support digital pattern generation. In the same manner as analog output, the digital pattern can be read from PC RAM or a file on the hard disk. Digital pattern generation is clocked in the same four modes as described with analog output.

The *ultra low-latency digital output mode* allows a digital output to be updated based on the level of an analog, digital or counter input. In this mode, the user associates a digital output bit with a specific input, and specifies the level of the input where the digital output changes state. The response time in this mode is dependent on the number of input channels being scanned, and can typically be in the range of 2 to 20 μ sec.

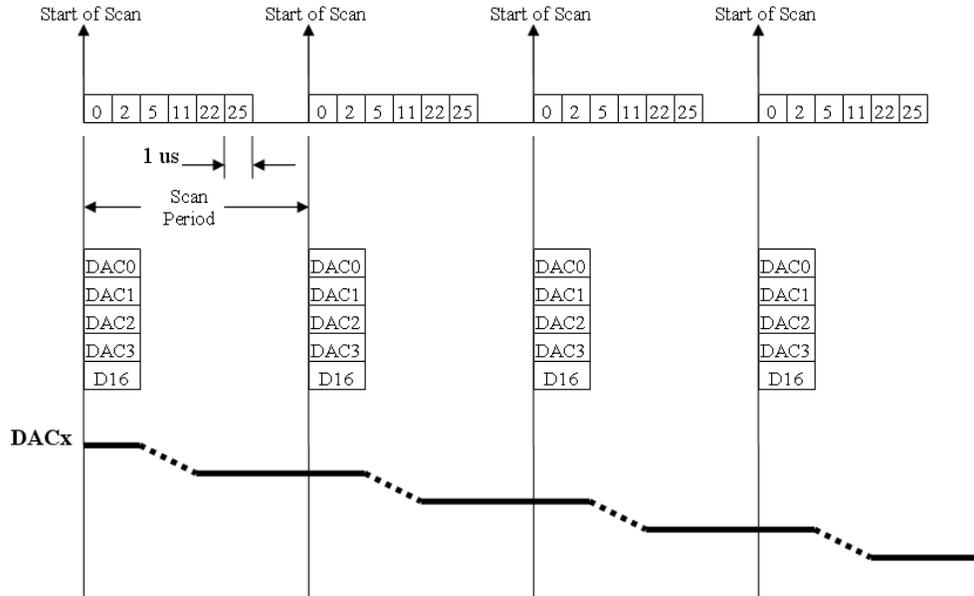


Reference Note:

For detailed information regarding low latency control outputs, see Chapter 6.

Example 5: Analog channel scanning of voltage inputs and streaming analog outputs

The figure below shows a simple acquisition. The scan is programmed pre-acquisition and is made up of 6 analog channels (Ch0, Ch2, Ch5, Ch11, Ch22, Ch25.) Each of these analog channels can have a different gain. The acquisition is triggered and the samples stream to the PC via USB2. Each analog channel requires one microsecond of scan time therefore the scan period can be no shorter than 6 us for this example. The scan period can be made much longer than 6 us, up to 19 hours. The maximum scan frequency is one divided by 6us or 166,666 Hz.



This example has all 4 DACs being updated and the 16-bits of digital IO. These updates are performed at the same time as the acquisition pacer clock (also called the scan clock.) All 4 DACs and the 16-bits of pattern digital output are updated at the beginning of each scan. Note that the DACs will actually take up to 4 us after the start of scan to settle on the updated value. This is due to the amount of time to shift the digital data out to the DACs plus the actual settling time of the digital to analog conversion.

The data for the DACs and pattern digital output comes from a PC-based buffer. The data is streamed across the USB2 bus to the Personal Daq/3000.

It is possible to update the DACs and pattern digital output with the DAC pacer clock (either internally generated or externally applied.) In this case, the acquisition input scans are not synchronized to the analog outputs or pattern digital outputs. It is possible to synchronize everything (input scans, DACs, pattern digital outputs) to one clock. That clock can be either internally generated or externally applied.

Counter Inputs

Each Personal Daq/3000 Series module includes four 32-bit counters; and each of the four counters accepts frequency inputs up to 20 MHz. The high-speed counter channels can be configured on a per-channel basis. Possible configurations include the following modes:

- Counter
- Period
- Pulse width
- Time between edges
- Multi-axis quadrature encoder

The counters can concurrently monitor time periods, frequencies, pulses, and other event driven incremental occurrences directly from encoders, pulse-generators, limit switches, proximity switches, and magnetic pick-ups.

As with all other inputs to the modules, the counter inputs can be read asynchronously under program control, or synchronously as part of an analog and digital scan group based on a programmable internal timer or an external clock source.

The modules support quadrature encoders with up to 2 billion pulses per revolution, 20 MHz input frequencies, and x1, x2, x4 count modes. With only A-phase and B-phase signals, 2 channels are supported. With A-phase, B-phase, and Z-index signals, 1 channel is supported.

Each input can be debounced from 500 ns to 25.5 ms (total of 16 selections) to eliminate extraneous noise or switch induced transients. Encoder input signals must be within -5V to +10V and the switching threshold is TTL (1.3V).



Reference Note:

For detailed information regarding the various counter modes refer to Chapter 5, *Counter Input Configuration Modes*.

Timer Outputs

Two 16-bit timer outputs are built into every 3000 series module. Each timer is capable of generating a different square wave with a programmable frequency in the range of 16 Hz to 1 MHz.

Example 6: Timer Outputs

Timer outputs are programmable square waves. The period of the square wave can be as short as 1us or as long as 65536 us. See the table below for some examples.

Divisor*	Timer Output Frequency	Related Equations
0	1 MHz	$F = 1 \text{ MHz} / (\text{Divisor} + 1)$ $\text{Divisor} = (1 \text{ MHz} / F) - 1$
99	10 kHz	
999	1 kHz	
4999	200 Hz	
9999	100 Hz	
65535	Turns Timer OFF*	

* The divisor range is 0 to 65535. For Setpoint Operation 65535 turns the timer off. In Asynchronous Write, 65535 results in a timer output frequency of 15.259 Hz.

There are 2 timer outputs that can generate different square waves. The timer outputs can be updated asynchronously at any time. Both timer outputs can also be updated during an acquisition as the result of setpoints applied to analog or digital inputs. See the section on pattern detection setpoints for more information and examples.

Multiple Personal Daqs

Multiple modules can be operated synchronously. This is done by designating one as the master. The other modules [slaves] are synchronized to the master by the pacer clock which is externally routed to the designated slave units.

For two or more Personal Daqs to be operated synchronously:

- (1) Use coax (or twisted-pair wire) to either (a) connect the APCR signals together,
or (b) connect the DPCR signals together.
- (2) Connect Digital Common [of each Personal Daq] to one of the twisted pairs,
or to the shield of the coax.

Software

Included with the /3000 Series is a complete set of drivers and example programs for the most popular programming languages and software packages. Driver support includes Visual Basic®, C/C++, LabVIEW®, DASYPac®, and MATLAB®. DaqCOM™ provides Windows®-based ActiveX/COM-based programming tools for Microsoft® Visual Studio® and Visual Studio.NET®. Also included with the /3000 Series is new DaqView™ software, a comprehensive Out-of-the-Box™ application that enables set-up, data logging, and real-time data viewing without existing programming skills. Optional DaqView/Pro also adds features such as direct-to-Excel® enhancements, FFT analysis, statistics, etc. DaqView software provides Out-of-the-Box™, quick and easy set up and collection of data.

Daq devices have software options capable of handling most applications. Three types of software are available:

- ready-to-use graphical programs, e.g., DaqView, DaqViewXL, and post acquisition data analysis programs such as PostView, DIAdem, and eZ-PostView
- drivers for third-party, icon-driven software such as DASYPac and LabView
- various language drivers to aid custom programming using API

Ready-to-use programs are convenient for fill-in-the-blank applications that do not require programming for basic data acquisition and display:

- DaqView is a Windows-based program for basic set-up and data acquisition. DaqView lets you select desired channels, gains, transducer types (including thermocouples), and a host of other parameters with a click of a PC's mouse. DaqView lets you stream data to disk and display data in numerical or graphical formats. PostView is a post-acquisition waveform-display program within DaqView.
- ViewXL/Plus allows you to interface directly with Microsoft Excel to enhance data handling and display. Within Excel you have a full-featured Daq control panel and all the data display capabilities of Excel.
- Post acquisition data analysis programs, e.g., PostView, DIAdem, and eZ-PostView, typically allow you to view and edit post-acquisition data.
- The Daq Configuration control panel allows for interface configuration, testing, and troubleshooting.

Each Daq system comes with an Application Programming Interface (API). API-language drivers include C/C++ and Visual Basic. The latest software is a 32-bit version API.



Reference Notes:

- The software documents for: *DaqView*, *ViewXL*, and *Post Acquisition Data Analysis* are not included as part of the hardcopy manual, but are available in PDF version. See the PDF Note, below.
- Programming topics are covered in the *Programmer's User Manual* (1008-0901). As a part of product support, this manual is automatically loaded onto your hard drive during software installation. The default location is the Programs directory, which can be accessed through the Windows Desktop.

PDF Note: During software installation, Adobe® PDF versions of user manuals will automatically install onto your hard drive as a part of product support. The default location is in the **Programs** group, which can be accessed from the *Windows Desktop*. Refer to the PDF documentation for details regarding both hardware and software.

A copy of the Adobe Acrobat Reader® is included on your CD. The Reader provides a means of reading and printing the PDF documents. Note that hardcopy versions of the manuals can be ordered from the factory.

- Overview 2-1
- Pinout for Personal Daq/3000 Series Modules 2-2
- PDQ30 Analog Expansion Option 2-3
- Connecting for Single-Ended or Differential 2-5

CAUTION



Turn off power to all devices connected to the system before connecting cables. Electrical shock or damage to equipment can result even under low-voltage conditions.

CAUTION

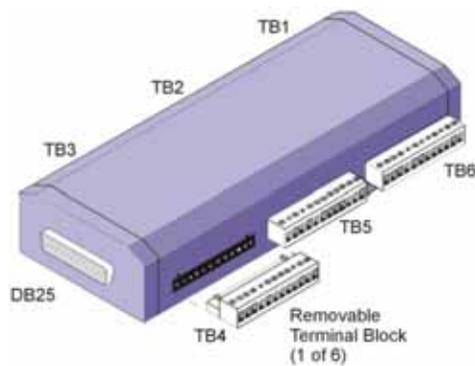


The discharge of static electricity can damage some electronic components. Semiconductor devices are especially susceptible to ESD damage. You should always handle components carefully, and you should never touch connector pins or circuit components unless you are following ESD guidelines in an appropriate ESD controlled area. Such guidelines include the use of properly grounded mats and wrist straps, ESD bags and cartons, and related procedures.

Overview

Personal Daq/3000 Series modules communicate to the host PC via USB cable. Each module has 6 removable blocks to provide convenient screw-terminal connections for all signal I/O. A DSUB25F connector allows for expansion via an optional PDQ30 module, either through direct connection or indirectly via a CA-96A cable.

Pinouts for the Personal Daq/3000 Series modules follow. In addition, use of the optional PDQ30 analog expansion module is discussed, and a pinout provided.



*Terminal Block Orientation for Personal Daq/3000 Series**

***Note:** Terminal Block Orientation for PDQ30 is different.

Pinout for Personal Daq/3000 Series Modules

USB2.0 Edge of Module

TB1	Analog Common		Digital Common		TB6
	DAC0 (Note 1)		Digital	CH 0	
	DAC1 (Note 1)		Digital	CH 1	
	DAC2 (Note 1)		Digital	CH 2	
	DAC3 (Note 1)		Digital	CH 3	
	Analog Common		Digital	CH 4	
	Self Calibration		Digital	CH 5	
	Signal Ground		Digital	CH 6	
	Digital Common		Digital	CH 7	
	TTL Trigger		Digital Common		
	DPCR (DAC Pacer Clock I/O)		Timer 0 (TMR0)		
	APCR (A/D Pacer Clock I/O)		Timer 1 (TMR 1)		

TB2	Analog Common		Digital Common		TB5
	CH 0 / CH 0 HI	Analog	Digital	CH 0	
	CH 8 / CH 0 LO	Analog	Digital	CH 1	
	Analog Common		Digital	CH 2	
	CH 1 / CH 1 HI	Analog	Digital	CH 3	
	CH 9 / CH 1 LO	Analog	Digital	CH 4	
	Analog Common		Digital	CH 5	
	CH 2 / CH 2 HI	Analog	Digital	CH 6	
	CH 10 / CH 2 LO	Analog	Digital	CH 7	
	Analog Common		Digital Common		
	CH 3 / CH 3 HI	Analog	Counter 0 (CNT0)		
	CH 11 / CH 3 LO	Analog	Counter 1 (CNT1)		

TB3	Analog Common		Digital Common		TB4
	CH 4 / CH 4 HI	Analog	Digital	CH 0	
	CH 12 / CH 4 LO	Analog	Digital	CH 1	
	Analog Common		Digital	CH 2	
	CH 5 / CH 5 HI	Analog	Digital	CH 3	
	CH 13 / CH 5 LO	Analog	Digital	CH 4	
	Analog Common		Digital	CH 5	
	CH 6 / CH 6 HI	Analog	Digital	CH 6	
	CH 14 / CH 6 LO	Analog	Digital	CH 7	
	Analog Common		Digital Common		
	CH 7 / CH 7 HI	Analog	Counter 2 (CNT2)		
	CH 15 / CH 7 LO	Analog	Counter 3 (CNT3)		

DSUB25 Edge of Module

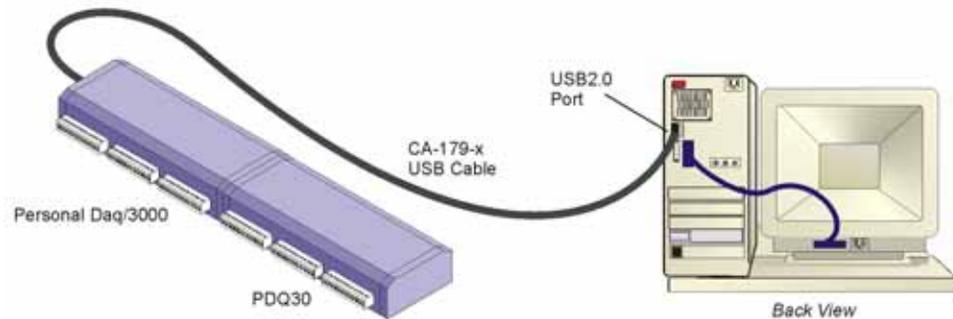
Note 1: Personal Daq/3000 includes DAC0 and DAC1; Personal Daq/3001 includes DAC0, DAC1, DAC2, and DAC3; Personal Daq/3005 has no DACs.

Note 2: Personal Daq/3000 Series devices can measure 16 channels of voltage or 8 channels of temperature. Temperature measurement requires the use of differential mode.

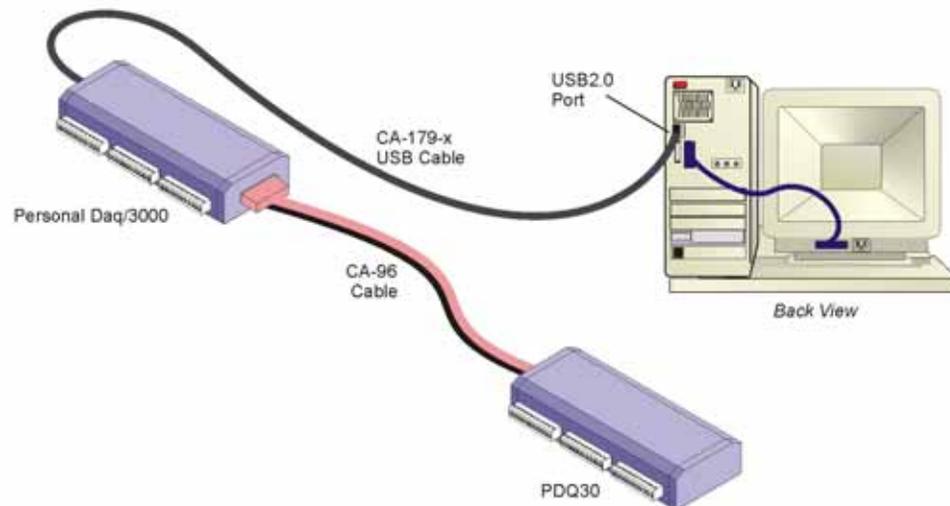
PDQ30 Analog Expansion Option

PDQ30 is an optional analog expansion module that, when connected to a Personal Daq/3000 series device, adds an additional 48 analog inputs. Refer to PDQ30 specifications sheet for channel input specifications.

Personal Daq/3000 Series modules can connect to a PDQ30, directly via DB25 connector or indirectly via a CA-96A cable. When connected directly, i.e., DB25 to DB25, two small clips (included) are used to hold the modules together.



Direct Connection of Personal Daq/3000 and PDQ30



Connection of Personal Daq/3000 and PDQ30 via a CA-96A Expansion Cable

CAUTION



PDQ30 is not to be connected to a live device! Turn off power to the host PC and externally connected equipment prior to connecting cables or signal lines. Electric shock or damage to equipment can result even under low-voltage conditions.



Take ESD precautions (packaging, proper handling, grounded wrist strap, etc.)

Ensure modules do not come into contact with foreign elements such as oils, water, and industrial particulate.

1. Ensure power is removed from all device(s) to be connected.
2. Observe ESD precautions when handling the module and making connections.
3. PDQ30's DB25 connector connects to a Personal Daq/3000 Series module DB25 connector either directly or via a CA-96A cable. Refer to the above figures.
4. Refer to the Declaration of Conformity in regard to meeting CE requirements.

Pinout for PDQ30

DSUB25 Edge of PDQ30 Module

TB1	Analog Common		Analog	CH 63 / CH 31 LO	TB6	
	CH 16 / CH 8 HI	Analog		Analog		CH 55 / CH 31 HI
	CH 24 / CH 8 LO	Analog		Analog Common		
	Analog Common			Analog		CH 62 / CH 30 LO
	CH 17 / CH 9 HI	Analog		Analog		CH 54 / CH 30 HI
	CH 25 / CH 9 LO	Analog		Analog Common		
	Analog Common			Analog		CH 61 / CH 29 LO
	CH 18 / CH 10 HI	Analog		Analog		CH 53 / CH 29 HI
	CH 26 / CH 10 LO	Analog		Analog Common		
	Analog Common			Analog		CH 60 / CH 28 LO
	CH 19 / CH 11 HI	Analog		Analog		CH 52 / CH 28 HI
	CH 27 / CH 11 LO	Analog		Analog Common		
TB2	Analog Common		Analog	CH 59 / CH 27 LO	TB5	
	CH 20 / CH 12 HI	Analog		Analog		CH 51 / CH 27 HI
	CH 28 / CH 12 LO	Analog		Analog Common		
	Analog Common			Analog		CH 58 / CH 26 LO
	CH 21 / CH 13 HI	Analog		Analog		CH 50 / CH 26 HI
	CH 29 / CH 13 LO	Analog		Analog Common		
	Analog Common			Analog		CH 57 / CH 25 LO
	CH 22 / CH 14 HI	Analog		Analog		CH 49 / CH 25 HI
	CH 30 / CH 14 LO	Analog		Analog Common		
	Analog Common			Analog		CH 56 / CH 24 LO
	CH 23 / CH 15 HI	Analog		Analog		CH 48 / CH 24 HI
	CH 31 / CH 15 LO	Analog		Analog Common		
TB3	Analog Common		Analog	CH 47 / CH 23 LO	TB4	
	CH 32 / CH 16 HI	Analog		Analog		CH 39 / CH 23 HI
	CH 40 / CH 16 LO	Analog		Analog Common		
	Analog Common			Analog		CH 46 / CH 22 LO
	CH 33 / CH 17 HI	Analog		Analog		CH 38 / CH 22 HI
	CH 41 / CH 17 LO	Analog		Analog Common		
	Analog Common			Analog		CH 45 / CH 21 LO
	CH 34 / CH 18 HI	Analog		Analog		CH 37 / CH 21 HI
	CH 42 / CH 18 LO	Analog		Analog Common		
	Analog Common			Analog		CH 44 / CH 20 LO
	CH 35 / CH 19 HI	Analog		Analog		CH 36 / CH 20 HI
	CH 43 / CH 19 LO	Analog		Analog Common		

Note: PDQ30 can measure 48 channels of voltage or 24 channels of temperature. Temperature measurement requires the use of differential mode.



Reference Note:
For PDQ30 specifications, refer to chapter 7.

Connecting for Single-Ended or Differential

Voltage signals can be connected using the Single-Ended method. In the following figure voltage source V1 is connected to Channel 0 and to analog common; and voltage source V2 is connected to Channel 8 and to analog common.

The figure also shows voltage V3 resulting from a thermocouple. In this case differential mode is being used. The high line from the thermocouple is shown connected to Channel 1 HI and the low (negative) side is connected to Channel 1 LO. Notice that Channel 1 LO uses the same screw terminal connection as CH 9.



In Personal Daq/3000 Series and PDQ30 applications, thermocouples should only be connected in differential mode. Connecting thermocouples in single-ended mode can cause noise and false readings.

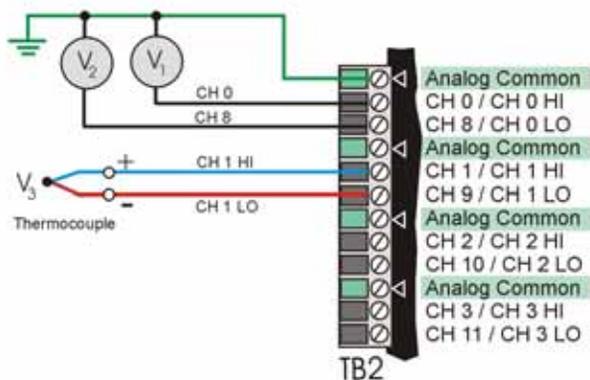


Personal Daq/3000 Series and PDQ30 devices do not have open thermocouple detection.

Thermocouple wires are to be connected in *differential mode* only.

Differential connection is made as follows:

- the red thermocouple wire connects to the channel's Low (L) connector.
- the other color wire connects to the channel's High (H) connector.



Single-Ended (V1 and V2) and Differential (V3) Connections to Analog Input Channels



Reference Note:

Appendix A, *Signal Modes and System Noise*, contains additional information.



Notes

Overview3-1
CE Standards and Directives 3-1
Safety Conditions3-2
Emissions/Immunity Conditions3-2

Overview

CE standards were developed by the European Union (EU) dating from 1985 and include specifications both for safety and for EMI emissions and immunity. Now, all affected products sold in EU countries must meet such standards. Although not required in the USA, these standards are considered good engineering practice since they enhance safety while reducing noise and ESD problems.

In contracted and in in-house testing, most products met the required specifications. Those products not originally in compliance were redesigned accordingly. In some cases, alternate product versions, shield plates, edge guards, special connectors, or add-on kits are required to meet CE compliance.



CE-compliant products bear the “CE” mark and include a *Declaration of Conformity* stating the particular specifications and conditions that apply. The test records and supporting documentation that validate the compliance are kept on file at the factory.

CE Standards and Directives

The electromagnetic compatibility (EMC) directives specify two basic requirements:

1. The device must not interfere with radio or telecommunications.
2. The device must be immune from electromagnetic interference from RF transmitters, etc.

The standards are published in the *Official Journal of European Union* under direction of CENELEC (European Committee for Electrotechnical Standardization). The specific standards relevant to Daq equipment are listed on the product’s Declaration of Conformity and include: CISPR22:1985; EN55022:1988 (Information Technology Equipment, Class A for commercial/industrial use); and EN50082-1:1992 for various categories of EMI immunity.

The safety standard that applies to Daq products is EN 61010-1 : 1993 (*Safety Requirements for Electrical Equipment for Measurement, Control, and Laboratory Use, Part 1: General Requirements*).

Environmental conditions include the following:

- indoor use
- altitude up to 2000 m
- temperature 5°C to 40°C (41°F to 104°F)
- maximum relative humidity 80% for temperatures up to 31°C (87.8°F) decreasing linearly to 50% relative humidity at 40°C (104°F)
- mains supply voltage fluctuations not to exceed $\pm 10\%$ of the nominal voltage
- other supply voltage fluctuations as stated by the manufacturer
- transient overvoltage according to installation categories (overvoltage categories) I, II and III
For mains supply, the minimum and normal category is II
- pollution degree I or II in accordance with IEC 664

For clarification, terms used in some Declarations of Conformity include:

- **pollution degree:** any addition of foreign matter, solid, liquid or gaseous (ionized gases) that may produce a reduction of dielectric strength or surface resistivity. **Pollution Degree I** has no influence on safety and implies: the equipment is at operating temperature with non-condensing humidity conditions; no conductive particles are permitted in the atmosphere; warm-up time is sufficient to avert any condensation or frost; no hazardous voltages are applied until completion of the warm-up period. **Pollution Degree II** implies the expectation of occasional condensation.
- **overvoltage (installation) category:** classification with limits for transient overvoltage, dependent on the nominal line voltage to earth. **Category I** implies signals without high transient values. **Category II** applies to typical mains power lines with some transients.

Safety Conditions

Users must comply with all relevant safety conditions in the user's manual and the Declarations of Conformity. This manual and the associated hardware make use of the following Warning and Caution symbols.

If you see either of these symbols on a product, carefully read the related information and be alert to the possibility of personal injury.



This warning symbol is used in this manual or on the equipment to warn of possible injury or death from electrical shock under noted conditions.



This warning/caution symbol is used to warn of possible personal injury or equipment damage under noted conditions.

Personal Daq products contain no user-serviceable parts; refer all service to qualified personnel. The specific safety conditions for CE compliance vary by product; but general safety conditions include:

- The operator must observe all safety cautions and operating conditions specified in the documentation for all hardware used.
- The host computer and all connected equipment must be CE compliant.
- All power must be off to the device and externally connected equipment before internal access to the device is permitted.
- Isolation voltage ratings: do not exceed documented voltage limits for power and signal inputs. All wire insulation and terminal blocks in the system must be rated for the isolation voltage in use. Voltages above 30 Vrms or ± 60 VDC must not be applied if any condensation has formed on the device.
- Current and power use must not exceed specifications. Do not defeat fuses or other over-current protection.

Emissions/Immunity Conditions

The specific immunity conditions for CE compliance vary by product; but general immunity conditions include:

- Cables must be shielded, braid-type with metal-shelled connectors. Input terminal connections are to be made with shielded wire. The shield should be connected to the chassis ground with the hardware provided.
- The host computer must be properly grounded.
- In low-level analog applications, some inaccuracy is to be expected when I/O leads are exposed to RF fields or transients over 3 or 10 V/m as noted on the Declaration of Conformity.



The DaqCal.exe calibration utility does not support Personal Daq/3000 Series devices at present. Please contact the factory for the latest calibration information concerning these products.

Every range of a Personal Daq/3000 Series device is calibrated at the factory using a digital NIST traceable calibration method. This method works by storing a correction factor for each range on the unit at the time of calibration. The user can adjust the calibration of the board while it is installed in the acquisition system without destroying the factory calibration. This is accomplished by having 3 distinct calibration tables in the on-board EPROM.

The user can select any of the three cal tables provided [factory, user, or self-cal tables] by API call or from within software. Self-cal can be performed automatically via the included software and without the use of external hardware or instruments. Self-cal derives its traceability through an on-board reference which has a stability of 0.005% per year.

Note that a 2-year calibration period is recommended for Personal Daq/3000 Series modules.

Using a Temperature Calibrator

The Personal Daq/3000 Series module provides accurate and repeatable temperature measurements across a wide range of operating conditions. However, all instrumentation is subject to drift with time and with ambient temperature change. If the ambient temperature of the operating environment is below 18°C or above 28°C, or if the product is near or outside its calibration interval, then the absolute accuracy may be improved through the use of an external temperature calibrator.

A temperature calibrator is a temperature simulation instrument that allows selection of thermocouple type and temperature. For proper operation, it must be connected to the Personal Daq/3000 Series module with the same type thermocouple wire and connector that is used in normal testing. The calibrator then generates and supplies a voltage corresponding to that which would be generated by the TC type [at the associated temperature].

The temperature selected on the calibrator will be dictated by the nature of normal testing. 0°C is usually the best choice. Calibrators are the most accurate at this setting, and the connecting thermocouple wire will contribute very little error at this temperature. However, if the dynamic range of the normal testing is, for example, 100°C to 300°C, a selection of 200°C may give better results. In either case, the level of adjustment is determined by comparing the unit reading to the selected calibrator temperature. For example, if the calibrator is set to 0°C output, and the Personal Daq/3000 Series module reads 0.3°C, then an adjustment of *minus* 0.3°C is required. That is, the adjustment value is determined by subtracting the Personal Daq module's reading from the calibrator setting.

To implement the adjustment in DaqView:

1. Ensure that the acquisition process is turned off.
2. Click on the cell in the Units column for the channel that is connected to the calibrator. The engineering units pull-down menu above the grid becomes active.
3. Click on the down arrow and select the "mx+b" option. This option allows post-acquisition mathematical manipulation.
4. For the example adjustment, enter -0.3 for "b." The channel under calibration will now read 0°C.

Note that this adjustment is a mathematical operation only, and in no way alters the hardware calibration of the product. Moreover, it operates on a per channel basis, with the settings for a given channel having no influence on any other channels.



Notes

Tips for Making High-Speed Counter Measurements (> 1 MHz) 5-1

Debounce Module 5-1

Terms Applicable to Counter Modes.....5-5

Counter Options 5-5

Counter/Totalize Mode 5-6

Period Mode 5-8

Pulsewidth Mode 5-11

Timing Mode 5-13

Encoder Mode 5-15

Note: Each of the high-speed, 32-bit counter channels can be configured for counter, period, pulse width, time between edges, or encoder modes.



Tips for Making High-Speed Counter Measurements (> 1 MHz)

- Use coax or twisted-pair wire. Connect one side to Digital Common.
- If the frequency source is tolerant, parallel-terminate the coax (or twisted-pair) with a 50 ohm or 100 ohm resistor at the terminal block.
- The amplitude of the driving waveform should be as high as possible without violating the over-voltage specification.
- To ensure adequate switching, waveforms should swing at least 0V to 5V and have a high slew rate.

Debounce

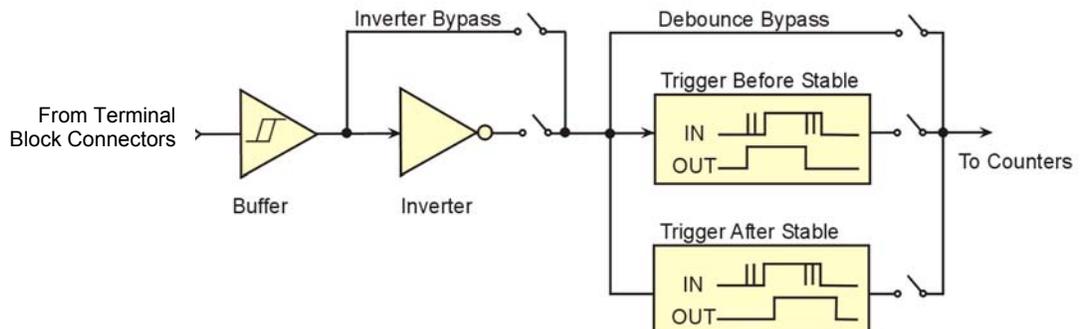
Each channel’s output can be debounced with 16 programmable debounce times from 500 ns to 25.5 ms. The debounce circuitry eliminates switch-induced transients typically associated with electro-mechanical devices including relays, proximity switches, and encoders.

From the following illustration we can see that there are two debounce modes, as well as a debounce bypass. In addition, the signal from the buffer can be inverted before it enters the debounce circuitry. The inverter is used to make the input rising-edge or falling-edge sensitive.

Edge selection is available with or without debounce. In this case the debounce time setting is ignored and the input signal goes straight from the inverter [or inverter bypass] to the counter module.

There are 16 different debounce times. In either debounce mode, the debounce time selected determines how fast the signal can change and still be recognized.

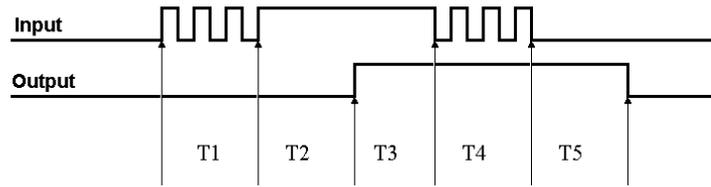
The two debounce modes are “trigger after stable” and “trigger before stable.” A discussion of the two modes follows.



Debounce Model

Trigger After Stable Mode

In the “Trigger After Stable” mode, the output of the debounce module will not change state until a period of stability has been achieved. This means that the input has an edge and then must be stable for a period of time equal to the debounce time.



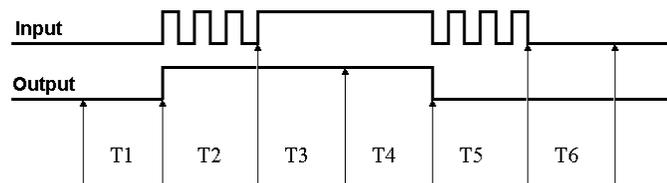
Debounce Module – Trigger After Stable Mode

The following time periods (T1 through T5) pertain to the above drawing. In Trigger After Stable mode, the input signal to the debounce module is required to have a period of stability after an incoming edge, in order for that edge to be accepted (passed through to the counter module.) The debounce time for this example is equal to T2 and T5.

- T1** – In the example above, the input signal goes high at the beginning of time period T1 but never stays high for a period of time equal to the debounce time setting (equal to T2 for this example.)
- T2** – At the end of time period T2, the input signal has transitioned high and stayed there for the required amount of time, therefore the output transitions high. If the Input signal never stabilized in the high state long enough, no transition would have appeared on the output and the entire disturbance on the input would have been rejected.
- T3** – During time period T3 the input signal remained steady. No change in output is seen.
- T4** – During time period T4, the input signal has more disturbances and does not stabilize in any state long enough. No change in the output is seen.
- T5** – At the end of time period T5, the input signal has transitioned low and stayed there for the required amount of time, therefore the output goes low.

Trigger Before Stable Mode

In the “Trigger Before Stable” mode, the output of the debounce module immediately changes state, but will not change state again until a period of stability has passed. For this reason the mode can be used to detect glitches.



Debounce Module – Trigger Before Stable Mode

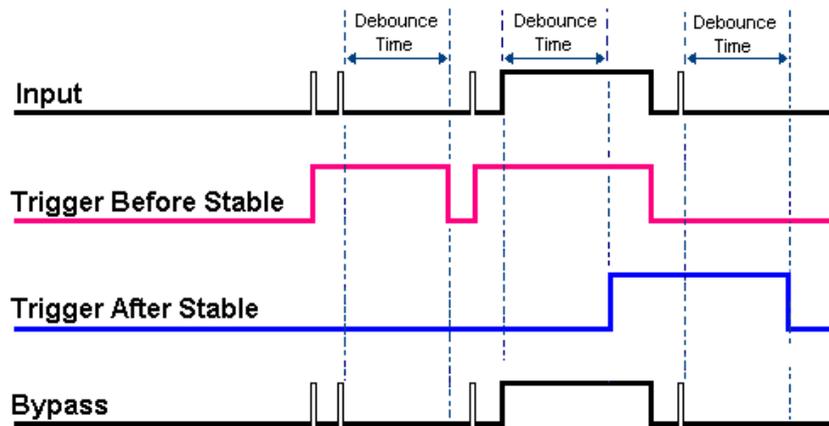
The following time periods (T1 through T6) pertain to the above drawing.

- T1** – In the illustrated example, the **Input** signal is low for the debounce time (equal to T1); therefore when the input edge arrives at the end of time period T1 it is accepted and the **Output** (of the debounce module) goes high. Note that a period of stability must precede the edge in order for the edge to be accepted.

- T2** – During time period T2, the input signal is not stable for a length of time equal to T1 (the debounce time setting for this example.) Therefore, the output stays “high” and does not change state during time period T2.
- T3** – During time period T3, the input signal is stable for a time period equal to T1, meeting the debounce requirement. The output is held at the high state. This is the same state as the input.
- T4** – At anytime during time period T4, the input can change state. When this happens, the output will also change state. At the end of time period T4, the input changes state, going low, and the output follows this action [by going low].
- T5** – During time period T5, the input signal again has disturbances that cause the input to not meet the debounce time requirement. The output does not change state.
- T6** – After time period T6, the input signal has been stable for the debounce time and therefore any edge on the input after time period T6 will be immediately reflected in the output of the debounce module.

Mode Comparison

The following example shows how the two modes interpret the same input signal (which exhibits glitches). Notice that the *Trigger Before Stable* mode will recognize more glitches than the *Trigger After Stable* mode. Use the *bypass* option to achieve maximum glitch recognition.

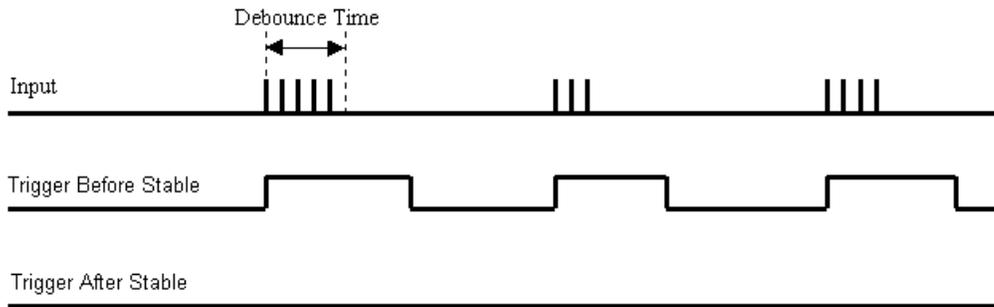


Example of Two Debounce Modes Interpreting the Same Signal

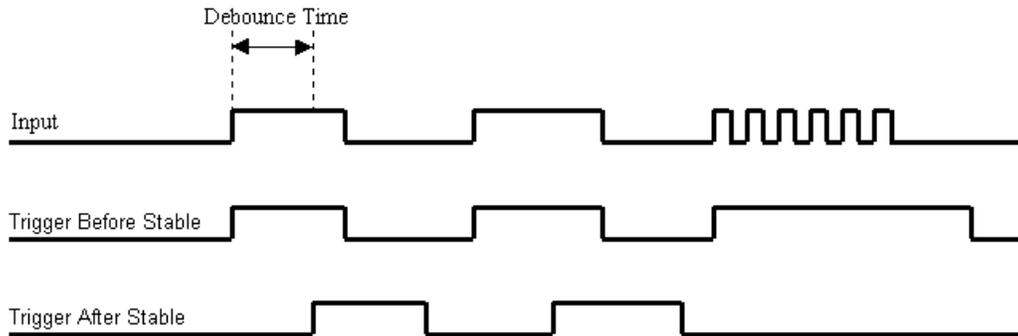
Debounce times should be set according to the amount of instability expected in the input signal. Setting a debounce time that is too short may result in unwanted glitches clocking the counter. Setting a debounce time too long may result in an input signal being rejected entirely. Some experimentation may be required to find the appropriate debounce time for a particular application.

To see the effects of different debounce time settings, simply view the analog waveform along with the counter output. This can be done by connecting the source to an analog input.

Use trigger before stable mode when the input signal has groups of glitches and each group is to be counted as one. The trigger before stable mode will recognize and count the first glitch within a group but reject the subsequent glitches within the group if the debounce time is set accordingly. The debounce time should be set to encompass one entire group of glitches as shown in the following diagram.



Trigger after stable mode behaves more like a traditional debounce function: rejecting glitches and only passing state transitions after a required period of stability. Trigger after stable mode is used with electro-mechanical devices like encoders and mechanical switches to reject switch bounce and disturbances due to a vibrating encoder that is not otherwise moving. The debounce time should be set short enough to accept the desired input pulse but longer than the period of the undesired disturbance as shown in the diagram below.



Terms Applicable to Counter Modes

The following terms and definitions are provided as an aid to understanding counter modes.

Gating: Any counter can be gated by the mapped channel. When the mapped channel is high, the counter will be allowed to count, when the mapped channel is low, the counter will not count but hold its value.

Mapped Channel: A mapped channel is one of 4 signals that can get multiplexed into a channel's counter module. The mapped channel can participate with the channel's input signal by gating the counter, clearing the counter, etc. The 4 possible choices for the mapped channel are the 4 input signals (post debounce).

Start of Scan: The start of scan is a signal that is internal to the 3000 Series module. It signals the start of a scan group and therefore pulses once every scan period. It can be used to clear the counters and latch the counter value into the acquisition stream.

Terminal Count: This signal is generated by the counter value. There are only two possible values for the terminal count: 65,535 for a 16-bit counter (Counter Low); and 4,294,967,295 for a 32-bit counter (Counter High). The terminal count can be used to stop the counter from rolling over to zero.

Ticksize: The ticksize is a fundamental unit of time and has four possible settings: 20.83ns, 208.3ns, 2083ns, 20833ns. For measurements that require a timebase reference like period or pulsewidth, the ticksize is the basic unit of time. Ticksize is derived from the period of the 48 MHz system clock. The count value returned in the scan is the number of ticks that make up the time measurement.

Counter Options

The following mode options are available with the /3000 Series module and are detailed in the upcoming pages.

A separate block diagram has been created for each mode. Note that the **OPT** numbers relate to sections of the block diagrams.

Counter/Totalize Mode (see page 6):

- OPT0:** Selects *totalize* or *clear on read* mode.
- OPT1:** Determines if the counter is to *rollover* or "*stop at the top.*"
- OPT2:** Determines whether the counter is 16-bits (Counter Low); or 32-bits (Counter High).
- OPT3:** Determines which signal latches the counter outputs into the data stream back to the module. Start of scan or mapped channel.
- OPT4:** Allows the mapped channel to gate the counter.
- OPT5:** Allows the mapped channel to decrement the counter.
- OPT6:** Allows the mapped channel to increment the counter.

Period Mode (see page 8):

- OPT[1:0]:** Determines the number of periods to time, per measurement (1, 10, 100, 1000).
- OPT2:** Determines whether the period is to be measured with a 16-bit (Counter Low); or 32-bit (Counter High).
- OPT4:** Allows the mapped channel to gate the counter.
- OPT6:** Allows the mapped channel to be measured for periods.

Pulsewidth Mode (see page 11):

- OPT2:** Determines whether the pulsewidth is to be measured with a 16-bit counter (Counter Low); or a 32-bit counter (Counter High).
- OPT4:** Allows the mapped channel to gate the counter.
- OPT6:** Allows the mapped channel to be measured for pulsewidth.

Timing Mode (see page 13).

- OPT2:** Determines whether the time is to be measured with a 16-bit counter (Counter Low); or a 32-bit counter (Counter High).

Encoder Mode (see page 15).

OPT[1:0]: Determines the encoder measurement mode: 1X, 2X, or 4X.

OPT2: Determines whether the counter is 16-bits (Counter Low); or 32-bits (Counter High).

OPT3: Determines which signal latches the counter outputs into the data stream going back to the module. Start of scan or mapped channel.

OPT4: Allows the mapped channel to gate the counter.

OPT5: Allows the mapped channel to clear the counter for Z reference.

Counter/Totalize Mode



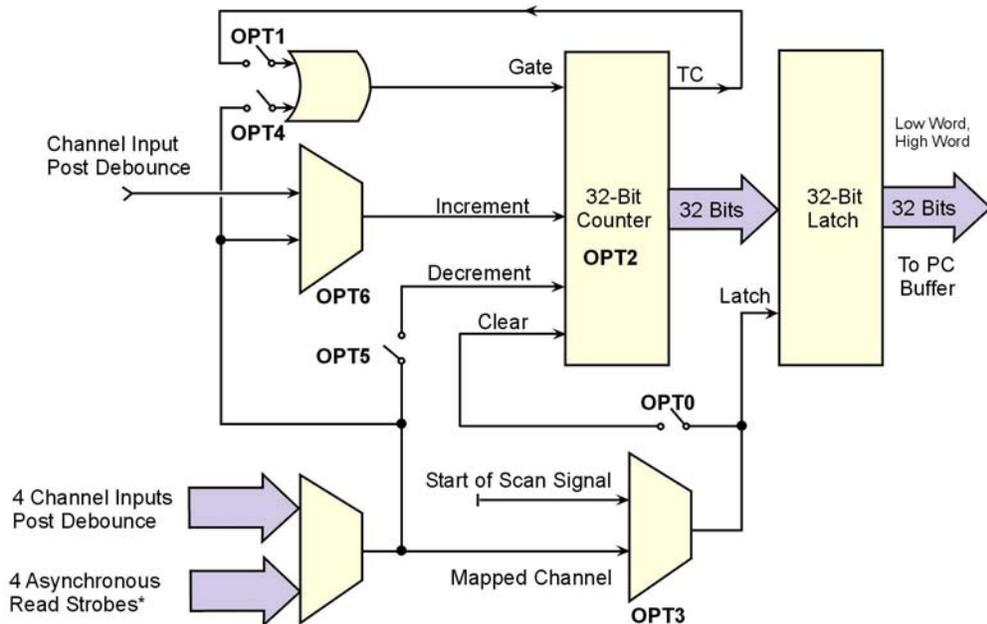
TIP: When using a counter for a trigger source, it is a good idea to use a pre-trigger with a value of at least 1. The reason is that all counters start at zero with the initial scan; and there will be no valid reference in regard to rising or falling edge. Setting a pre-trigger to 1 or more ensures that a valid reference value is present, and that the first trigger will be legitimate.

The *counter mode* allows basic use of a 32-bit counter. While in this mode, the channel's input can only increment the counter upward. When used as a 16-bit counter (Counter Low), one channel can be scanned at the 12 MHz rate. When used as a 32-bit counter (Counter High), two sample times are used to return the full 32-bit result. Therefore a 32-bit counter can only be sampled at a 6 MHz maximum rate. If only the upper 16 bits of a 32-bit counter are desired then that upper word can be acquired at the 12 MHz rate.

The first scan of an acquisition always zeroes all counters. It is usual for all counter outputs to be latched at the beginning of each scan; however, there is an option to change this. A second channel, referred to as the **“mapped” channel**, can be used to latch the counter output. The mapped channel can also be used to:

- **gate the counter**
- **increment the counter**
- **decrement the counter**

The mapped channel can be any of the 4 counter input channels (post-debounce), or any of the four asynchronous read strobes. When a counter is not in the scan it can be asynchronously read with, or without, *clear on read*. The asynchronous read-signals strobe when the lower 16-bits of the counter are read by software. The software can read the counter's high 16-bits at a later time, after reading the lower 16-bits. The full 32-bit result reflects the timing of the first asynchronous read strobe.



Counter/Totalize Mode

*There is one asynchronous read strobe for each of the four counter channels.

An explanation of the various counter options, depicted in the previous figure, follows.

COUNTER: OPT0: This selects *totalize* or *clear on read* mode.

Totalize Mode – The counter counts up and rolls over on the 16-bit (Low Counter) boundary, or on the 32-bit (High Counter) boundary. See OPT2 in regard to choosing 16-bit or 32-bit counters.

Clear On Read Mode – The counter is cleared at the beginning of every scan or synchronous read; and the final value of the counter [the value just before it was cleared] is latched and returned to the module.

COUNTER: OPT1: This determines if the counter is to *rollover* or “*stop at the top.*”

Rollover Mode - The counter continues to count upward, rolling over on the 16-bit (Counter Low) boundary, or on the 32-bit (Counter High) boundary. See OPT2 in regard to choosing 16-bit or 32-bit counters.

Stop at the Top Mode - The counter will stop at the top of its count. The top of the count is FFFF for the 16-bit option (Counter Low), and FFFFFFFF for the 32-bit option (Counter High).

COUNTER: OPT2: Determines whether the counter is **16-bits** or **32-bits** (Counter Low, or Counter High, respectively). This only matters when the counter is using the “stop at the top” option, otherwise this option is inconsequential.

COUNTER: OPT3: **Determines which signal latches the counter outputs** into the data stream back to the module. Normally, the start of scan signal latches the counter outputs at the beginning of every scan; but an option is to have the mapped signal latch the counter outputs. This mapped-signal option allows a second signal to control the latching of the count data. This allows the user to know the exact counter value when an edge is present on another channel. This also allows the counters to be asynchronously read.

COUNTER: OPT4: Allows the **mapped channel to gate the counter** if desired. When the mapped channel is **high**, the counter is enabled. When the mapped channel is **low**, the counter is disabled (but holds the count value). The mapped channel can be any other input channel.

COUNTER: OPT5: Allows the **mapped channel to decrement the counter**. With this option the input channel [for the counter] will increment the counter. The mapped channel can be used to decrement the counter.

COUNTER: OPT6: Allows the **mapped channel to increment the counter** instead of the main channel. This option allows the counter to be used with any other input channel (post-debounce). If the channel’s input is used elsewhere, for example, gating another counter, the counter for this channel does not need to go unused.

Asynchronously Reading These Counters

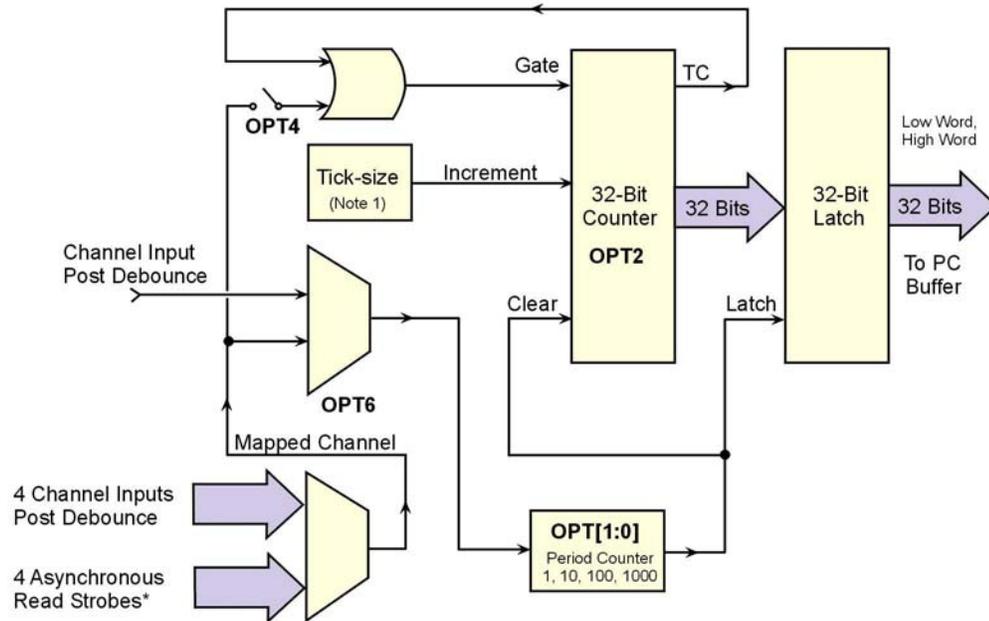
If the counter is in asynchronous mode the *clear on read* mode is available. The counter’s lower 16-bit value should be read first. This will latch the full 32-bit result and clear the counter. The upper 16-bit value can be read after the lower 16-bit value. Also, counters can only be asynchronously read in modes that allow the mapped channel to latch the data, i.e., Counter and Encoder modes. However, it is possible for the user to use that read strobe as a mapped channel elsewhere, if desired. For example, the read strobe could be used to increment or decrement the counter.

Period Mode



TIP: When using a counter for a trigger source, it is a good idea to use a pre-trigger with a value of at least 1. The reason is that all counters start at zero with the initial scan; and there will be no valid reference in regard to rising or falling edge. Setting a pre-trigger to 1 or more ensures that a valid reference value is present, and that the first trigger will be legitimate.

This mode allows for period measurement of the channel input. The measurement period is the time from edge-to-edge, either both rising or both falling. Period data is latched as it becomes available and the data is logged by the /3000 Series module at the scan rate. Therefore, if the scan period is much faster than the input waveform, there will be a great deal of repetition in the period values. This repetition is due to the fact that updates take place only when another full period becomes available.



Period Mode

*There is one asynchronous read strobe for each of the four counter channels.

Note 1: Tick-sizes are: 20.83ns, 208.3ns, 2083ns, and 20833ns, derived from the 48 MHz system clock.

An example: One channel's acquired data might be: 0,0,0,0,80,80,80,80,79,79,79,79,81,81,81,81,..... This data represents the number of ticksize intervals counted during the period measurement. The first value(s) returned will be zero since the counters are cleared at the beginning of the acquisition. The data comes in sets of four since the scan period is about one-fourth as long as the input channel's period. Every time the period measurement is latched from the counter, the counter is immediately cleared and begins to count the time for the subsequent period.

If the scan period is a lot slower than the input period, the acquired data will be missing some periods. To obtain greater resolution, you can increase the scan period, or use an averaging option (see OPT[1:0]).

The data returned is interpreted as time measured in ticks. There are four timebase settings: 20.83 ns, 208.3 ns, 2083 ns, and 20833 ns. These are often referred to as tick-sizes. The /3000 Series module uses a 48 MHz, 50 ppm oscillator as a timing source. The tick sizes are derived from 1 period, 10 periods, 100 periods, or 1000 periods of the 48 MHz clock.

PERIOD: OPT[1:0]: Determines the **number of periods to time, per measurement**. This makes it possible to *average out jitter* in the input waveform, sampling error, noise, etc. There are four options:

- (1) The channel's measurement is latched every time one complete period has been observed.
- (2) The channel's measurement is latched every time that 10 complete periods have been observed. The value that gets returned is equal to 10 consecutive periods of the input channel.
- (3) The number returned is 100 consecutive periods.
- (4) The number returned is 1000 consecutive periods.

PERIOD: OPT2: Determines whether the period is to be measured with a **16-bit** (Counter Low), or **32-bit** (Counter High) counter. Since period measurements always have the "stop at the top" option enabled, this option dictates whether the measurement has a range of 0 to 65535 ticks or 0 to 4,294,967,295 ticks.

PERIOD: OPT4: Allows the **mapped channel to gate the counter** if desired. When the mapped channel is **high**, the counter is enabled. When the mapped channel is **low**, the counter is disabled, but still holds the count value. The mapped channel can be any other input channel.

PERIOD: OPT6: This allows a mapped channel's period to be measured, instead of the input channel. The mapped channel can be any other input channel (post debounce). This option allows the counter to be used with any other input channel (post-debounce). If the channel's input is used elsewhere, for example, gating another counter, the counter for this channel does not need to go unused.

Period and Frequency Accuracy

The /3000 Series module can measure the period of any input waveform. It does this by counting the integral number of "ticks" that make up the period, the data returned will always be time measured in "ticks." The error in each data sample will come from two sources: the sampling error caused by not being able to count a partial "tick"; and the 3000 Series module's internal timebase inaccuracy. The module's internal timebase has an absolute accuracy of 50 ppm. The sampling error will vary with input frequency, selected ticksize, and selected averaging mode. The absolute error is the "root-sum-of-squares" of the two independent error sources.

Many times the desired accuracy is much less than what the internal timebase is capable of. Other applications will require a more accurate period measurement and the effects of sampling error will have to be averaged out leaving only the inaccuracy associated with the internal timebase. Inaccuracy due to the internal timebase cannot be averaged out.

For period and frequency measurements, percent sampling error is equal to $100\%/(n+1)$ where $n=0$ to 65,535 for a 16-bit counter and $n=0$ to 4,294,967,295 for a 32-bit counter. For small count values, the sampling error is large and for large count values, the sampling error is small. If sampling error is to be less than 0.21%, n must be greater than 480 regardless of counter size.

Sampling error can also be reduced by averaging many samples together. Assuming the input signal is asynchronous to the module's internal timebase, sampling error can be divided by the square-root of the number of samples taken. The averaging can be done with PC-based software.

The device has the ability to measure 1, 10, 100 or 1000 periods, dividing the sampling error by 1, 10, 100, or 1000. This is done within the Personal Daq/3000 Series circuitry and may eliminate the need for any averaging to be done in the PC. For high accuracy on high frequency inputs, multiple period measurement and PC-based averaging can be done.

3000 Series devices have the ability to provide various frequency ranges that are based upon different ticksizes, averaging options, and counter size (16 bit or 32 bit values.) The frequency ranges are designed to fit a wide array of possible applications. Within each range, the sampling error decreases dramatically as the input period increases. The ranges will get smaller as required accuracy increases.

Upper 16-bits of the 32-bit counter		
Range (Hz)	Ticksize (nS)	Averaging Option
15u – 1500u	20833.333	1
150u – 15m	2083.333	1
1500u – 150m	208.333	1
15m – 1500m	20.833	1
150m – 15	20.833	10
1500m – 150	20.833	100
15 – 1500	20.833	1000

Lower 16-bits of the 32-bit counter		
Range (Hz)	Ticksize (nS)	Averaging Option
1 – 100	20833.333	1
10 – 1k	2083.333	1
100 – 10k	208.333	1
1k – 100k	20.833	1
10k – 1M	20.833	10
100k – 5M	20.833	100
1M – 5M	20.833	1000

Frequency Ranges for a 16-bit value, sampling error is less than 0.21%

Each frequency range given in the previous table-set can be exceeded. If the input waveform goes under-range by too much, the counter value will top out at 65535 indicating you have reached the lowest possible frequency that can be measured on that range. If the input waveform goes over range by too much, the counter will return values that are very coarse and have a lot of sampling error. The values returned will have a small number of counts for the period duration. If an input waveform cannot fit within one of the 16-bit ranges shown above or requires much higher accuracy, then a 32-bit range should be considered.

Full 32-bit Counter		
Range (Hz)	Ticksize (nS)	Averaging Option
15u – 100	20833.333	1
150u – 1k	2083.333	1
1.5m – 10k	208.333	1
15m – 100k	20.833	1
150m – 1M	20.833	10
1.5 – 5M	20.833	100
15 – 5M	20.833	1000

**Frequency Ranges for a 32-bit Value,
Sampling Error is Less than 0.21%**

The 32-bit ranges shown above are much wider than the 16-bit ranges, but also require the full 32-bit value to be returned. Since digital or counter channels do not take up any time in the scan period there is no disadvantage in reading a 32-bit counter versus a 16-bit counter. The 32-bit frequency ranges can also be exceeded with a loss of accuracy or topping out at 4,294,967,295 counts.

Some measurements will require the accuracy of an input waveform to be free of sampling error, having only the absolute accuracy of the internal timebase as the source of error. Sampling error can be averaged out to give the required result. In most cases, the 3000 Series device can perform the required averaging on the values before they are returned to the PC. The frequency ranges shown below will give a sampling error that is less than 10ppm or 1ppm.

Full 32-bit Counter <10 ppm		
Range (Hz)	Ticksize (nS)	Averaging Option
15u – 500m	20833.333	1
150u – 5	2083.333	1
1.5m – 50	208.333	1
15m – 500	20.833	1
150m – 5k	20.833	10
1.5 – 50k	20.833	100
15 – 500k	20.833	1000

Full 32-bit Counter <1 ppm		
Range (Hz)	Ticksize (nS)	Averaging Option
15u – 50m	20833.333	1
150u – 500m	2083.333	1
1.5m – 5	208.333	1
15m – 50	20.833	1
150m – 500	20.833	10
1.5 – 5k	20.833	100
15 – 50k	20.833	1000

**High Accuracy Frequency Ranges for a 32-bit Value
that has little sampling error (<10ppm, <1ppm)**

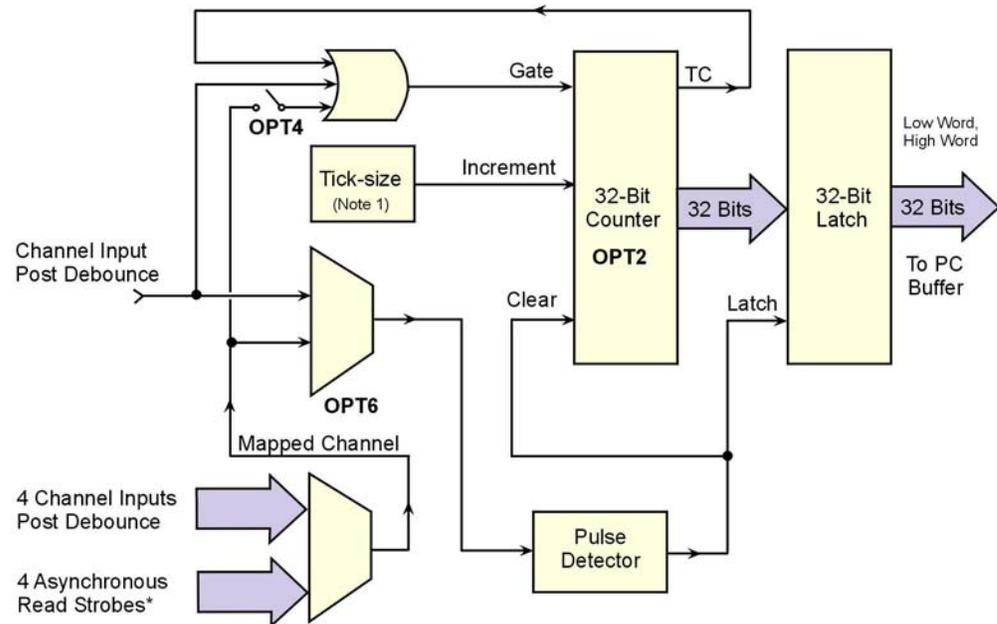
If the input frequency is required to have less than 1 ppm sampling error and is greater than 50kHz, use the 15– 50kHz, 1ppm range. The values returned will have sampling error that is greater than 1ppm but they can be averaged by the PC software to further reduce the sampling error.

Pulsewidth Mode



TIP: When using a counter for a trigger source, it is a good idea to use a pre-trigger with a value of at least 1. The reason is that all counters start at zero with the initial scan; and there will be no valid reference in regard to rising or falling edge. Setting a pre-trigger to 1 or more ensures that a valid reference value is present, and that the first trigger will be legitimate.

This mode provides a means to measure a channel's pulsewidth. The measurement is the time from the rising edge to the falling edge, or visa versa. The measurement will be either pulsewidth low, or pulsewidth high, depending upon the edge polarity set in the debounce module. Every time the pulsewidth measurement is latched from the counter, the counter is immediately cleared and enabled to count the time for the next pulsewidth. The pulsewidth measurements are latched as they become available.



Pulsewidth Mode

*There is one asynchronous read strobe for each of the four counter channels.

Note 1: Tick-sizes are: 20.83ns, 208.3ns, 2083ns, and 20833ns, derived from the 48 MHz system clock.

An example: one channel's acquired data might be: 0,0,0,0,80,80,80,80,79,79,79,79,81,81,81,81,... This data represents the number of ticksize intervals counted during the pulsewidth measurement. The first value(s) returned will be zero since the counters are cleared at the beginning of the acquisition. In this example the data comes in sets of four because the scan period is about one-fourth as long as the input channel's period. Every time the pulsewidth measurement is latched from the counter, the counter is immediately cleared and enabled to count time for the next pulsewidth.

If the scan period is much slower than the input period, then the acquisitions will miss some pulsewidths. Decreasing the scan period will increase the number of different pulsewidths received.

The data returned is interpreted as time measured in ticks. There are four timebase settings: 20.833 ns, 208.33 ns, 2.083 μ s, and 20.83 μ s. These are often referred to as tick-sizes. The 3000 Series module uses a 48 MHz, 50 ppm oscillator as a timing source.



Note! If the input signal has a poor slew rate the pulsewidth mode will provide variant results.

PULSEWIDTH: OPT2: Determines whether the pulsewidth is to be measured with a **16-bit** (Counter Low), or **32-bit** (counter High) counter. Since pulsewidth measurements always have the “stop at the top” option enabled, this option dictates whether the measurement has a range of 0 to 65535 ticks, or 0 to 4,294,967,295 ticks.

PULSEWIDTH: OPT4: Allows the **mapped channel to gate the counter**. When the mapped channel is **high**, the counter is enabled to count. When the mapped channel is **low**, the counter is disabled, but holds the count value. The mapped channel can be any other input channel.

PULSEWIDTH: OPT6: This allows the mapped channel’s pulsewidth to be measured instead of the input channel. The mapped channel can be any other input channel (post debounce). This option allows the counter to be used with any other input channel (post-debounce). If the channel’s input is used elsewhere, for example, gating another counter, the counter for this channel does not need to go unused.

Pulsewidth and Timing mode Accuracy

Personal Daq/3000 Series modules have the ability to measure the pulsewidth of an input and the time between any two edges on any two inputs. The time ranges are similar to those shown for period mode except that averaging is not available. The ranges given below reflect this.

Upper 16-bits of the 32-bit Counter		
Range (S)	Ticksize (nS)	Averaging Option
800 – 80000	20833.333	1
80 – 8000	2083.333	1
8 – 800	208.333	1
800m – 80	20.833	1

Lower 16-bits of the 32-bit Counter		
Range (S)	Ticksize (nS)	Averaging Option
10m – 1	20833.333	1
1m – 100m	2083.333	1
100u – 10m	208.333	1
10u – 1m	20.833	1

*Pulsewidth and Time Ranges for a 16-bit Value
Sampling error is less than 0.21%*

Full 32-bit Counter		
Range (S)	Ticksize (nS)	Averaging Option
10m – 80000	20833.333	1
1m – 8000	2083.333	1
100u – 800	208.333	1
10u – 80	20.833	1

*Pulsewidth and Time Ranges for a 32-bit Value
Sampling error is less than 0.21%*

Full 32-bit Counter <10 ppm		
Range (S)	Ticksize (nS)	Averaging Option
2 – 80000	20833.333	1
200m – 8000	2083.333	1
20m – 800	208.333	1
2m – 80	20.833	1

Full 32-bit Counter <1 ppm		
Range (S)	Ticksize (nS)	Averaging Option
20 – 80000	20833.333	1
2 – 8000	2083.333	1
200m – 800	208.333	1
20m – 80	20.833	1

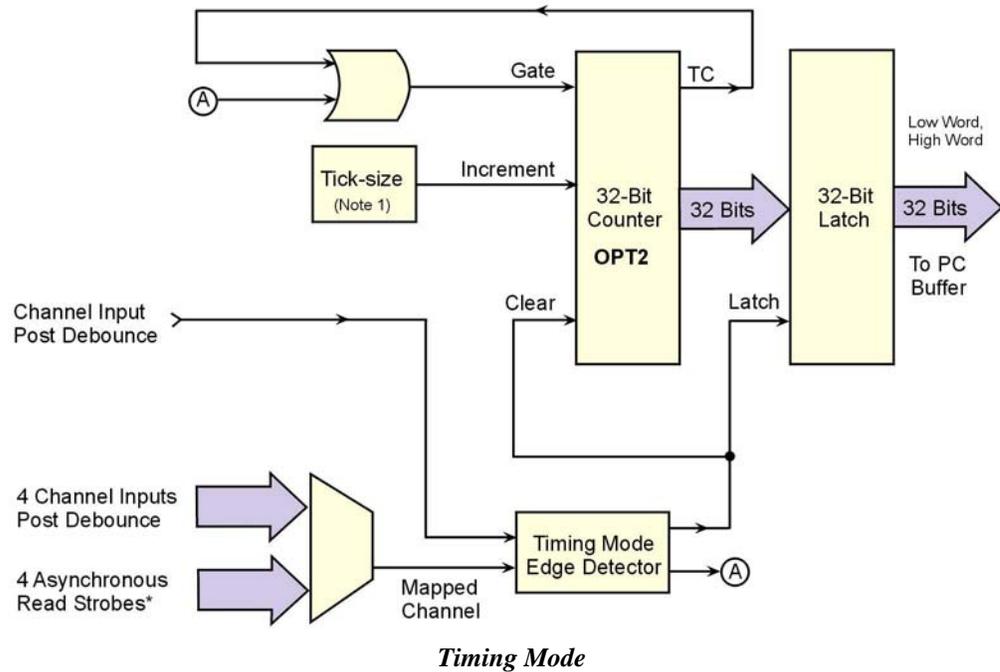
*High Accuracy Pulsewidth and Time Ranges for a 32-bit Value
that has little sampling error (<10ppm, <1ppm)*

Timing Mode



TIP: When using a counter for a trigger source, it is a good idea to use a pre-trigger with a value of at least 1. The reason is that all counters start at zero with the initial scan; and there will be no valid reference in regard to rising or falling edge. Setting a pre-trigger to 1 or more ensures that a valid reference value is present, and that the first trigger will be legitimate.

This mode provides a means of measuring time between two subsequent events, i.e., the edge of one channel with respect to the edge of another channel. The edge selection is done in each channel's debounce setup. Whenever the time measurement is latched from the counter, the counter is immediately cleared and enabled for accepting the subsequent time period, which starts with the next edge on the main channel.



*There is one asynchronous read strobe for each of the four counter channels.

Note 1: Tick-sizes are: 20.83ns, 208.3ns, 2083ns, and 20833ns, derived from the 48 MHz system clock.

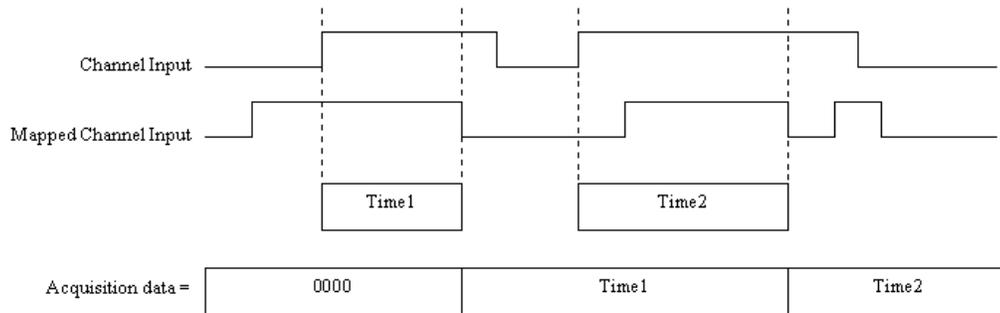
An Example of Timing Mode

The following example represents one channel in timing mode. The time desired is between the *rising edge* on the **input channel** and the *falling edge* on the **mapped channel**. Zeroes are returned, in the scan, until one complete time measurement has been taken. At that point, the value (time in ticks) is latched and logged by the /3000 Series device until the next time measurement has been completed. Rising edges on the input channel will clear the counter and falling edges on the mapped channel will latch the output of the counter at that time. If the scan period is much slower than the rate of time-frames coming [available on the two channels] then the data will miss some time-frames. The scan period can be decreased to capture more time-frames.

The data returned is interpreted as time measured in ticks. This data represents the number of ticksize intervals counted during the timing measurement. There are four timebase settings: 20.833 ns, 208.33 ns, 2.083 μ s, and 20.83 μ s. These are often referred to as tick-sizes. The 3000 Series device uses a 48 MHz, 50 ppm oscillator as a timing source.



If the input signal has a poor slew rate the timing mode will provide variant results, dependant upon the input switching threshold.



Example of One Channel in Timing Mode

TIMING: OPT2: This determines whether the time is to be measured with a **16-bit** (Counter Low), or **32-bit** (Counter High) counter. Since time measurements always have the “stop at the top” option enabled, this option dictates whether the measurement has a range of 0 to 65535 ticks or 0 to 4,294,967,295 ticks.

Encoder Mode



TIP: When using a counter for a trigger source, it is a good idea to use a pre-trigger with a value of at least 1. The reason is that all counters start at zero with the initial scan; and there will be no valid reference in regard to rising or falling edge. Setting a pre-trigger to 1 or more ensures that a valid reference value is present, and that the first trigger will be legitimate.

Introduction

Rotary shaft encoders are frequently used with CNC equipment, metal-working machines, packaging equipment, elevators, valve control systems, and in a multitude of other applications in which rotary shafts are involved.

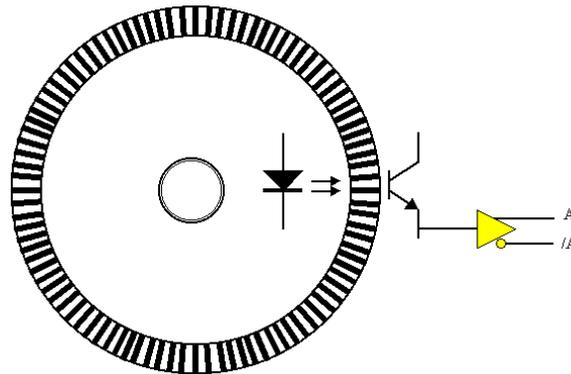
The *encoder mode* allows the 3000 Series module to make use of data from optical incremental quadrature encoders. When in the *encoder mode*, the Personal Daq accepts *single-ended* inputs. When reading phase A, phase B, and index Z signals, the /3000 Series device provides positioning, direction, and velocity data.



The Personal Daq/3000 Series module can only receive input from up to two encoders.

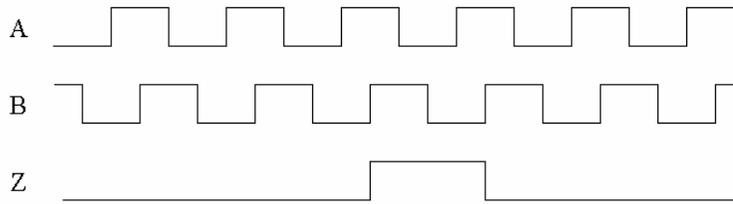
3000 Series Personal Daqs support quadrature encoders with a 16-bit (Counter Low), or a 32-bit (Counter High) counter, 20 MHz frequency, and x1, x2, and x4 count modes. With only phase A and phase B signals, 2 channels are supported; with phase A, phase B, and index Z signals, 1 channel is supported.

Quadrature encoders generally have 3 outputs: A, B, and Z. The A and B signals are pulse trains driven by an optical sensor inside the encoder. As the encoder shaft rotates, a laminated optical shield rotates inside the encoder. The shield has three concentric circular patterns of alternating opaque and transparent windows through which an LED will shine. There is one LED for each of the concentric circular patterns and likewise, one phototransistor. One phototransistor produces the A signal, another phototransistor produces the B signal and the last phototransistor produces the Z signal. The concentric pattern for A has 512 window pairs (or 1024, 4096, etc.)



The concentric pattern for B has the same number of window pairs as A except that the entire pattern is rotated by 1/4 of a window-pair. Thus the B signal will always be 90 degrees out of phase from the A signal. The A and B signals will pulse 512 times (or 1024, 4096, etc.) per complete rotation of the encoder.

The concentric pattern for the Z signal has only one transparent window and therefore pulses only once per complete rotation. Representative signals are shown in the following figure.

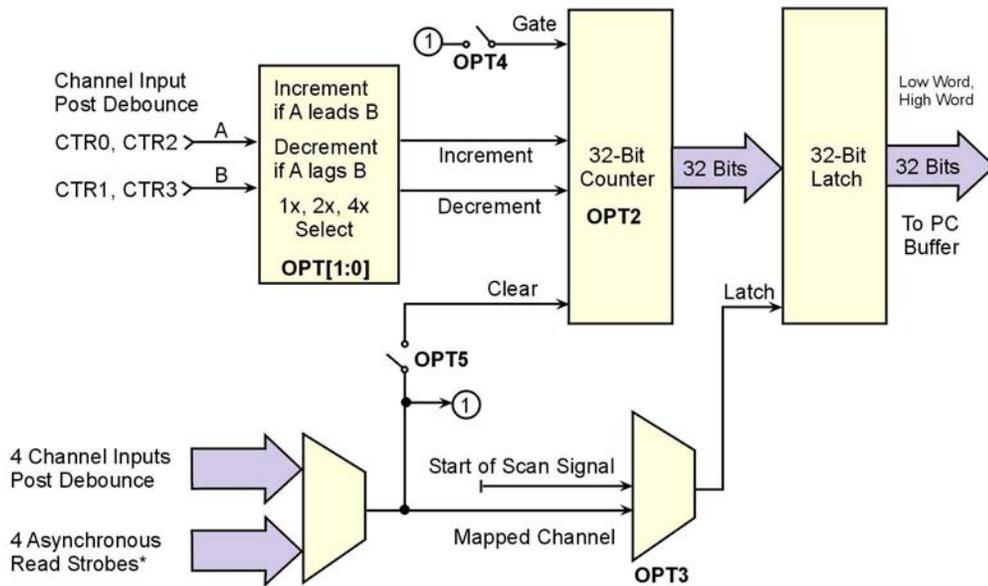


Representation of Quadrature Encoder Outputs: A, B, and Z

As the encoder rotates, the A (or B) signal is indicative of the distance the encoder has traveled. The frequency of A (or B) indicates the velocity of rotation of the encoder. If the Z signal is used to zero a counter (that is clocked by A) then that counter will give the number of pulses the encoder has rotated from its reference. The Z signal is a reference marker for the encoder. It should be noted that when the encoder is rotating clockwise (as viewed from the back), A will lead B and when the encoder is rotating counter-clockwise, A will lag B. If the counter direction control logic is such that the counter counts upward when A leads B and counts downward when A lags B, then the counter will give direction control as well as distance from the reference.

An Example of Encoder Accuracy

If there are 512 pulses on A, then the encoder position is accurate to within 360 degrees/512. Even greater accuracy can be obtained by counting not only rising edges on A but also falling edges on A, giving position accuracy to 360 degrees/1024. The ultimate accuracy is obtained by counting rising and falling edges on A and on B (since B also has 512 pulses.) This gives a position accuracy of 360 degrees/2048. These 3 different modes are known as 1X, 2X, and 4X. The 3000 Series module implements all of these modes and functions, as described in the following options.



Encoder Mode

*There is one asynchronous read strobe for each of the four counter channels.

ENCODER: OPT[1:0]: This determines the encoder measurement mode: 1X, 2X, or 4X.

ENCODER: OPT3: This determines which signal latches the counter outputs into the data stream going back to the /3000 Series device. Normally, the start of scan signal latches the counter outputs at the beginning of every scan. The other option is to have the mapped signal latch the counter outputs. This allows the user to have another signal control the latching of the count data, so the exact value of the counter is known when an edge is present on another channel.

ENCODER: OPT4: This allows the mapped channel to gate the counter if desired. When the mapped channel is high, the counter is enabled to count, when the mapped channel is low, the counter is disabled (but holds the count value.) The mapped channel can be any other input channel.

ENCODER: OPT5: This allows the mapped channel to clear the counter if desired. OPT5 implements the Z-function [described above], allowing the encoder reference to clear the counter. The counter is cleared on the rising edge of the mapped channel.

Encoder Wiring Diagrams

You can use up to two encoders with each 3000 Series device in your acquisition system. Each A and B signal can be made as a single-ended connection with respect to common ground.

Encoder wiring diagrams and example setup tables are included in the following pages; refer to them as needed.

For Single-ended Connections:

For single-ended applications, the connections made from the encoder to the 3000 Series device are as follows:

- Signals A, B, and Z connect to the Counter Inputs on the Personal Daq/3000 Series device.
- Each encoder ground connects to GND.



Differential applications are not supported.



For Open-Collector Outputs: External *pullup resistors* can be connected to the 3000 Series counter input terminal blocks. A pullup resistor can be placed between any input channel and the encoder power supply.

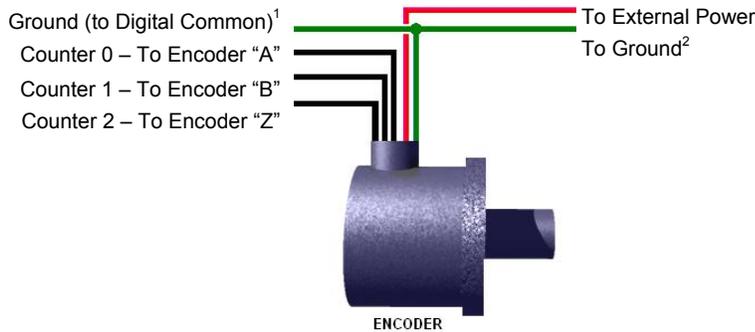
Choose a pullup resistor value based on the encoder's output drive capability and the input impedance of the 3000 Series module. Lower values of pullup resistors will cause less distortion but also cause the encoder's output driver to pull down with more current.

Wiring for 1 Encoder

The following figure illustrates connections for one encoder to a Personal Daq/3000 module.



The “A” signal must be connected to an even-numbered channel and the associated “B” signal must be connected to the next [higher] odd-numbered channel. For example, if “A” were connected to Counter 0, then “B” would be connected to Counter 1.



Encoder Connections to pins on the Personal Daq/3000

¹ The ground depicted at the left is associated with Digital Common on the Personal Daq/3000 Series module.

² The ground depicted at the right is associated with the external power source.

In addition to the previous figure, the following table indicates how to connect a single encoder to a 3000 Series device. Each signal (A, B, Z) can be connected as a single-ended connection with respect to the common ground. The encoder will need to be powered from an external power output (typically +5VDC). Connect the encoder’s power input to the power source and connect the return to digital common (GND) of that source.

The programming setup given below is just a representative of possible options.

Single Encoder – Programming Example Setup for Personal Daq/3000 Series Module		
Screw Terminal	Connects to:	Example Programming Setup
TB5, Terminal 2 Counter 0 (CNT0)	Encoder – A	Encoder Mode, 4X option, 16-bit counter, Latch on SOS, Map channel Clears the counter, set Map channel to CTR2.
TB5, Terminal 1 Counter 1 (CNT1)	Encoder – B	Period Mode, 1Xperiod option, 16-bit counter, Map channel doesn't gate, Ticksiz to 208.3 ns.
TB4, Terminal 2 Counter 2 (CNT2)	Encoder – Z	Counter in Totalize mode, stop-at-the-top, 16-bit counter.

If the encoder stops rotating, but is vibrating [due to the machine it is mounted to], the debounce feature can be used to eliminate false edges. An appropriate debounce time can be chosen and applied to each encoder channel. Refer to the *Debounce Module* section on page 5-1 for additional information regarding debounce times.

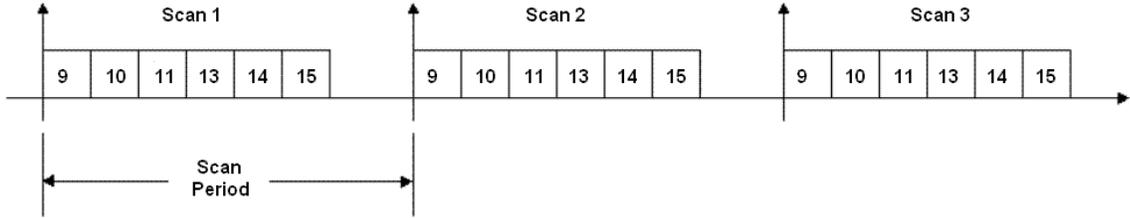
Relative position and *velocity* can be obtained from the encoder. However, during an acquisition, data that is relative to the Z-position cannot be obtained until the encoder locates the Z-reference.



During an acquisition, data that is relative to the Z-position cannot be obtained until the encoder locates the Z-reference.

Note that the number of Z-reference crossings can be tabulated. If the encoder was turning in only one direction, then the Z-reference crossings will equal the number of complete revolutions. This means that the data streaming to the PC will be *relative position*, $period = 1/velocity$, and *revolutions*.

A typical acquisition might take 6 readings off of the Personal Daq/3000 as illustrated below. The user determines the scan rate and the number of scans to take.



Personal Daq/3000 Series, Acquisition of Six Readings per Scan

Note: Digital channels do not take up analog channel scan time.

In general, the output of each channel's counter is latched at the beginning of each scan period (called the *start-of-scan*.) Every time the 3000 Series module receives a *start-of-scan* signal, the counter values are latched and are available to the unit.

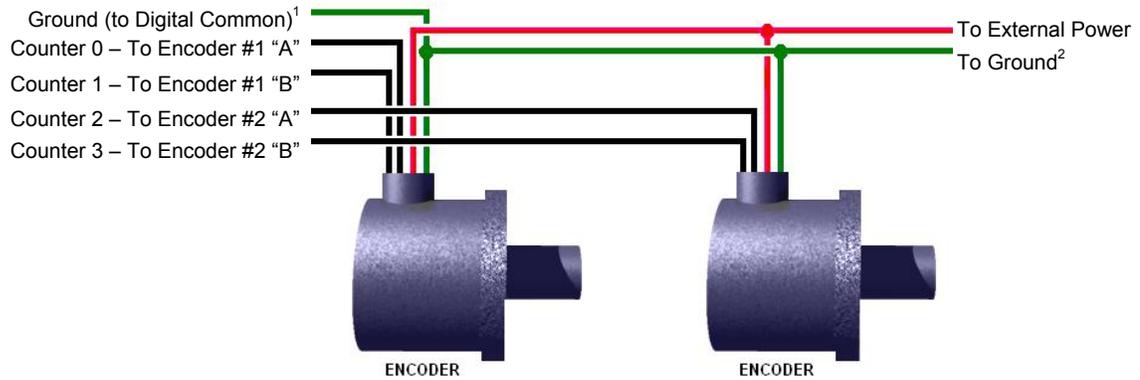
The Personal Daq clears all counter channels at the beginning of the acquisition. This means that the values returned during scan period 1 will always be zero. The values returned during scan period 2 reflect what happened during scan period 1.



The scan period defines the timing resolution for the Personal Daq/3000 Series. If you need a higher timing resolution, shorten the scan period.

Wiring for 2 Encoders

The following figure illustrates single-ended connections for two encoders. Differential connections are not applicable.



Two Encoders Connected to Personal Daq/3000

¹The ground depicted at the left is associated with Digital Common on the Personal Daq/3000 Series module.

²The ground depicted at the right is associated with the external power source.

Connect two encoders to the 3000 Series device as shown in the table below. Each signal (A, B) can be connected as a single-ended connection with respect to the common digital ground (GND). Both encoders will need powered from an external power source (typically +5VDC).

Connect each encoder's power input to the external power source. Connect the return to digital common (GND) on the same source. The programming setup given below is just one example. Other setups are possible.

Two Encoders – Programming Example Setup for Personal Daq/3000		
Screw Terminal	Connects to:	Example Programming Setup
TB5, Terminal 2 Counter 0 (CNT0)	Encoder #1 – A	Encoder Mode, 1X option, 16-bit counter, Latch on SOS
TB5, Terminal 1 Counter 1 (CNT1)	Encoder #1 – B	Period Mode, 1Xperiod option, 16-bit counter, Map channel doesn't gate, Ticksizes to 20833 ns
TB4, Terminal 2 Counter 2 (CNT2)	Encoder #2 – A	Encoder Mode, 2X option, 16-bit counter, Latch on SOS
TB4, Terminal 1 Counter 3 (CNT3)	Encoder #2 – B	Period Mode, 1Xperiod option, 16-bit counter, Map channel doesn't gate, Ticksizes to 2083.3 ns

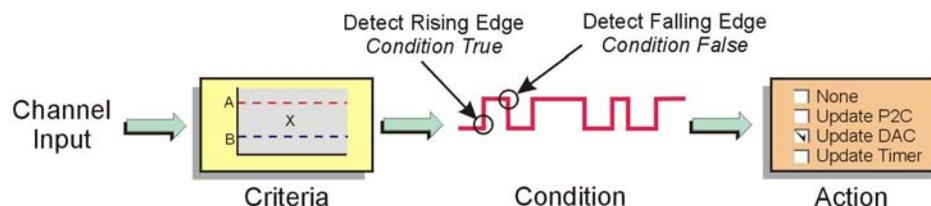
With the encoders connected in this manner there is no relative positioning information available on encoder #1 or #2 since there is no Z signal connection for either. Therefore only distance traveled and velocity can be measured for each encoder.

- Overview 6-1**
- Detecting Input Values 6-3**
- Controlling Analog, Digital, and Timer Outputs 6-4**
- P2C, DAC, or Timer Update Latency 6-6**
- More Examples of Control Outputs 6-7**
 - Detection on an Analog Input, DAC and P2C Updates 6-7
 - Detection on an Analog Input, Timer Output Updates 6-8
 - Using the Hysteresis Function 6-8
 - Using Multiple Inputs to Control One DAC Output 6-10
- The Setpoint Status Register 6- 11**

Overview

Personal Daq/3000 Series modules include a setpoint configuration feature which allows the user to individually configure up to 16 detection setpoints associated with channels within a scan group. Each detection setpoint can be programmed in the following ways:

- **Single Point referenced** – above, below, or equal to the defined setpoint
- **Window (dual point) referenced** – inside, or outside the window
- **Window (dual point) referenced, Hysterisis Mode** – outside the window high forces one output (designated “Output 2”; outside the window low forces another output, designated as “Output 1.”



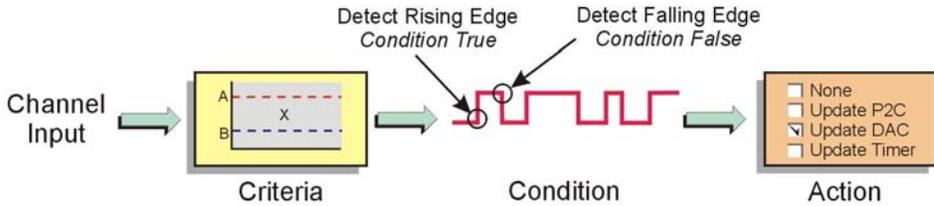
A digital detect signal is used to indicate when a signal condition is True or False, i.e., whether or not the signal has met the defined criteria. The detect signals themselves can be part of the scan group and can be measured as any other input channel; thus allowing real time data analysis during an acquisition.

Each setpoint can update the following, allowing for real time control based on acquisition data:

- **P2C digital output port with a data byte and mask byte**
- **analog outputs (DACs)**
- **timers**

The detection module looks at the 16-bit data being returned on a given channel and generates another signal for each channel with a setpoint applied: Detect1 for Channel 1, Detect2 for Channel 2, etc. These signals serve as data markers for each channel’s data. It doesn’t matter whether that data is volts, counts, period, pulsewidth, timing, or encoder position.

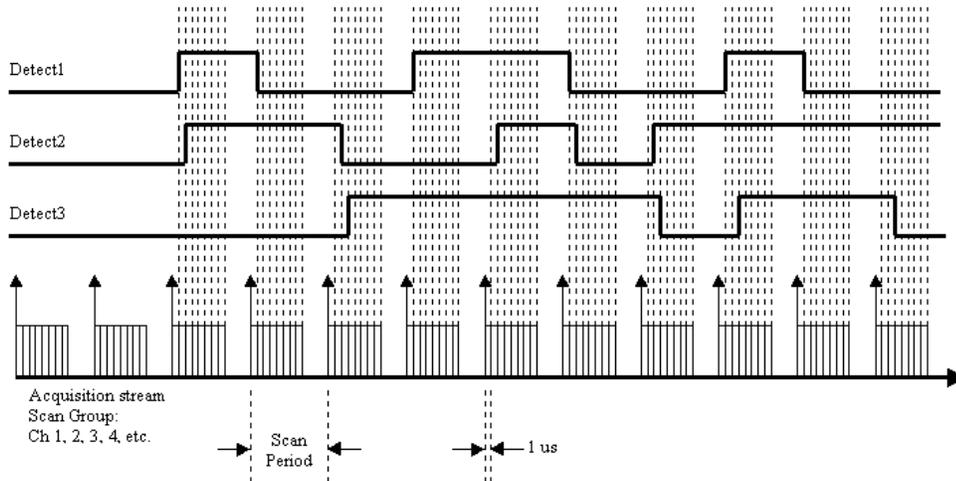
A channel’s detect signal will show a **rising edge** and will be **True (1)** when the channel’s data meets the setpoint criteria. The detect signal will show a **falling edge** and will be **False (0)** when the channel’s data does not meet the setpoint criteria. The true and false states, for each setpoint criteria, appear in the *Setpoint Status Register* (see page 6-11).



Criteria Input Signal is Equal to X		Action Driven by Condition
Compare X To:	Setpoint Definition:	Update Conditions:
Limit A or Limit B	<ul style="list-style-type: none"> Equal to A $X = A$ Below A (Choose 1) $X < A$ Above B $X > B$ 	True Only: If True, then Output Value 1; If False, then perform no action True and False: If True, then Output Value 1; If False, then Output Value 2
Window* (non-Hysteresis Mode)	<ul style="list-style-type: none"> Inside $B < X < A$ Outside (Choose 1) $B > X$; or $X > A$ 	True Only: If True, then Output Value 1; If False, then perform no action True and False: If True, then Output Value 1; If False, then Output Value 2
Window* (Hysteresis Mode)	<ul style="list-style-type: none"> Above A $X > A$ Below B $X < B$ <p>(Both conditions are checked when in Hysteresis Mode)</p>	Hysteresis Mode (Forced Update): If $X > A$ is True, then Output Value 2 until $X < B$ is True, then Output Value 1. If $X < B$ is True, then Output Value 1 until $X > A$ is True, then Output Value 2. This is saying: (a) If the input signal is outside the window "high", then Output Value 2 until the signal goes outside the window "low" and (b) if the signal is outside the window low, then Output Value 1 until the signal goes outside the window "high." There is no change to the detect signal while within the window.

* Value A defines the upper limit of the Window and Value B defines the low limit.

The detect signal has the timing resolution of the scan period as seen in the diagram below. The detect signal can change no faster than the scan frequency (1/scan period.)



Example Diagram of Detection Signals for Channels 1, 2, and 3

Each channel in the scan group can have one detection setpoint. There can be no more than 16 setpoints, in total, applied to channels within a scan group.

Detection setpoints act on 16-bit data only. Since the Personal Daq/3000 Series modules have 32-bit counters, data is returned 16-bits at a time. The lower word, the higher word or both lower and higher words can be part of the scan group. Each counter input channel can have 1 detection setpoint for the counter's lower 16-bit value and 1 detection setpoint for the counter's higher 16-bit value.

Detecting Input Values

All setpoints are programmed as part of the pre-acquisition setup, similar to setting up the analog path, debounce mode, or counter mode setup. Since each setpoint acts on 16-bit data, each has two 16-bit compare values: **Limit A** (High Limit) and **Limit B** (Low Limit). These limits define the setpoint window.

There are several possible conditions (criteria) and effectively 3 update modes, as can be seen in the following configuration summary.

Setpoint Configuration Summary

- ◇ **16-bit High Limit** Identified as “Limit A” in software
- ◇ **16-bit Low Limit** Identified as “Limit B” in software
- ◇ **Criteria:**

<i>Inside window</i>	Signal is below Limit A and Above Limit B
<i>Outside window</i>	Signal is above Limit A, or below Limit B
<i>Greater than value</i>	Signal is above Limit B, <i>Limit A is not used</i>
<i>Less than value</i>	Signal is below Limit A, <i>Limit B is not used</i>
<i>Equal to value</i>	Signal is equal to Limit A, <i>Limit B is not used</i> . Note that the <i>Equal to mode</i> is intended for use with counter or digital input channels [as the source channel]. See the TIP below.
<i>Hysteresis mode</i>	<i>Outside the window high</i> forces Output 2 until an <i>outside the window low</i> condition exists; then Output 1 is forced. Output 1 continues until an <i>outside the window high</i> condition exists. The cycle repeats as long as the acquisition is running in Hysteresis mode.

- ◇ **Update Mode:**
 - Update on True Only*
 - Update on True and False*
 - None - Do not update*
- ◇ **16-bit DAC value, P2C value, or Timer value when input meets criteria**
- ◇ **16-bit DAC value, P2C value, or Timer value when input does not meet criteria**
- ◇ **Type of Action:**
 - None*
 - Update P2C (see note)*
 - Update DACx*
 - Update Timerx*



By software default, P2C comes up as a digital input. If you want the P2C signal to be a digital output [in some initial state before an acquisition is started] and P2C is to be updated by set point criterion, then you must do an asynchronous write to P2C before the acquisition is started. The initial value will only be output if the asynchronous write to P2C has been performed.



DAC defaults are 0V. If an initial condition other than 0V is desired, you must do an asynchronous write to the associated DAC before the acquisition is started.



When using setpoints with triggers *other than* immediate, hardware analog, or TLL, the setpoint criteria evaluation will begin immediately upon arming the acquisition.



TIP: It is recommended that the “Equal to Limit A” mode only be used with counter or digital input channels as the channel source. If similar functionality is desired for analog channels, then the “Inside Window” mode should be used.

Controlling Analog, Digital, and Timer Outputs

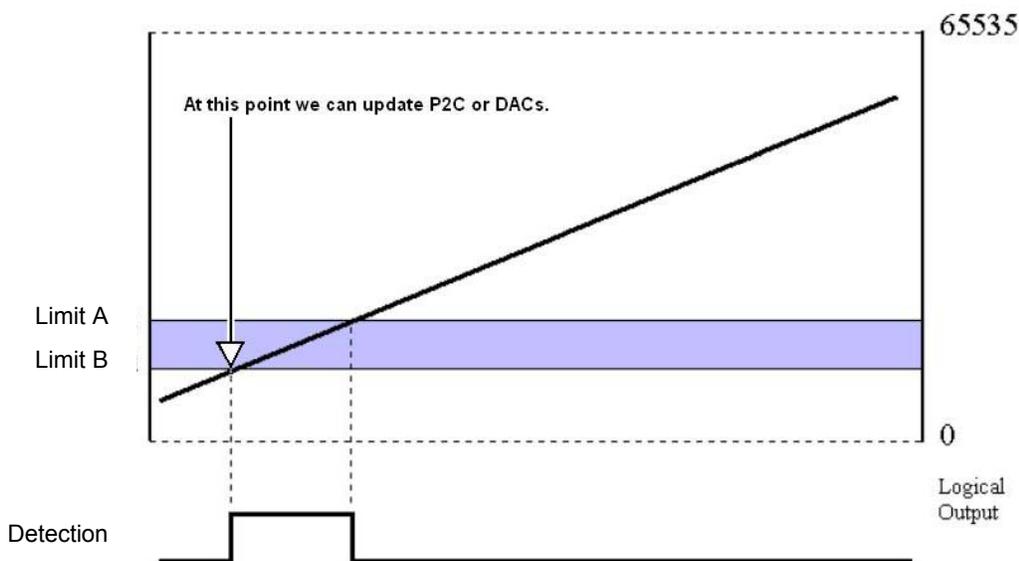
Each setpoint can be programmed with an 8-bit digital output byte and corresponding 8-bit mask byte. When the setpoint criteria has been met, the P2C digital output port can be updated with the given byte and mask. Alternately, each setpoint can be programmed with a 16-bit DAC update value, any one of the 4 DAC outputs can be updated in real time. Any setpoint can also be programmed with a timer update value.

In *hysteresis mode* each setpoint has two forced update values. Both update values can drive the same output target; i.e. DAC, timer, or P2C digital output port. *In hysteresis mode the outputs do not change when the input values are inside the window.* There is one update value that gets applied when the input values are less than the window and a different update value that gets applied when the input values are greater than the window.

Update on True and False uses two update values. There is one update value that gets applied when the specified criteria is met (True) and a different update value that gets applied when the specified criteria is not met (False). The update values can drive DACs, P2C, or timer outputs.

Example: Setpoint Detection on a Totalizing Counter

In the following figure Channel 1 is a counter in totalize mode. Two setpoints are used to define a point of change for Detect 1 as the counter counts upward. The detect output will be high when inside the window (greater than Limit B (the low limit) but less than Limit A (the high limit)). In this case, the Channel 1 setpoint is defined for the 16 lower bits of channel 1's 32-bit value. The P2C digital output port could be updated on a True condition (the rising edge of the Detection signal). Alternately, one of the DAC output channels, or timer outputs, could be updated with a value.



Channel 1 in Totalizing Counter Mode, Inside the Window Setpoint

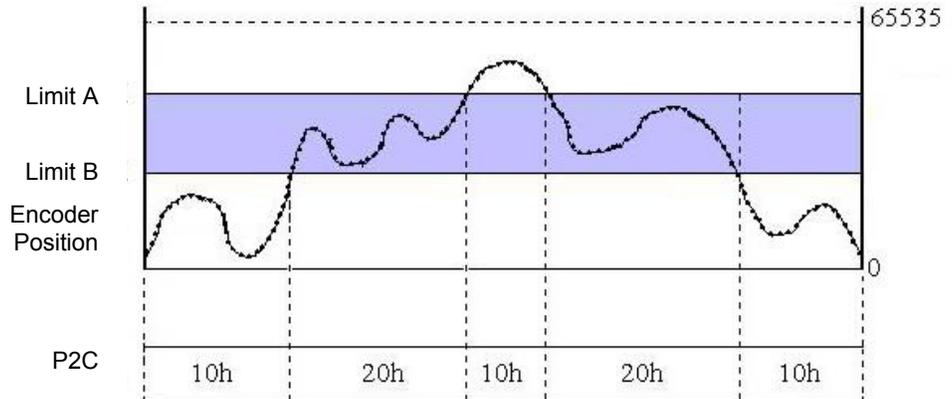
The detection circuit works on data that is put into the acquisition stream at the scan rate. This data is acquired according to the pre-acquisition setup (scan group, scan period, etc.) and returned to the PC. Counters are latched into the acquisition stream at the beginning of every scan. The actual counters may be counting much faster than the scan rate and therefore only every 10th, 100th, or nth count will show up in the acquisition data. Therefore it is possible to set a small detection window on a totalizing counter channel and have the detection setpoint “stepped over” since the scan period was too long. Even though the counter value stepped into and out of the detection window, the actual values going back to the PC may not. This is true no matter what mode the counter channel is in.

The setting of a detection window must be done with a scan period in mind. This applies to analog inputs and counter inputs. Quickly changing analog input voltages can step over a setpoint window if not sampled often enough.

There are three possible solutions for overcoming this problem:

- (1) The scan period could be shortened to give more timing resolution on the counter values or analog values
- (2) The setpoint window can be widened by increasing Limit A and/or lowering Limit B.
- (3) A combination of both solutions (1 and 2) could be made.

Example: Setpoint Detection on a Counter in Encoder Mode.



Example of a Counter in Encoder Mode

The figure above shows values pertaining to a Counter in Encoder Mode. The acquisition is started and 16-bit data [from the counter] streams into the PC at the scan rate. The 16-bit counter data is interpreted as the position from an encoder, which is connected to the counter inputs.

The update on *True and False* mode is being used. Thus, one value is output on P2C when the position is *outside of the window* (a value of 10h in the example); and a second value is output on P2C when the position is *inside the window* (a value of 20h in the example).

In the *True and False* mode, each setpoint has two update values. One of the two values is used to update the output target [DAC, P2C, or timer] when the input channel meets the setpoint criteria. The second value is used to update the same target when the condition is *false*.



By software default, P2C comes up as a digital input. If you want the P2C signal to be a digital output [in some initial state before an acquisition is started] and P2C is to be updated by set point criterion, then you must do an asynchronous write to P2C before the acquisition is started. The initial value will only be output if the asynchronous write to P2C has been performed.

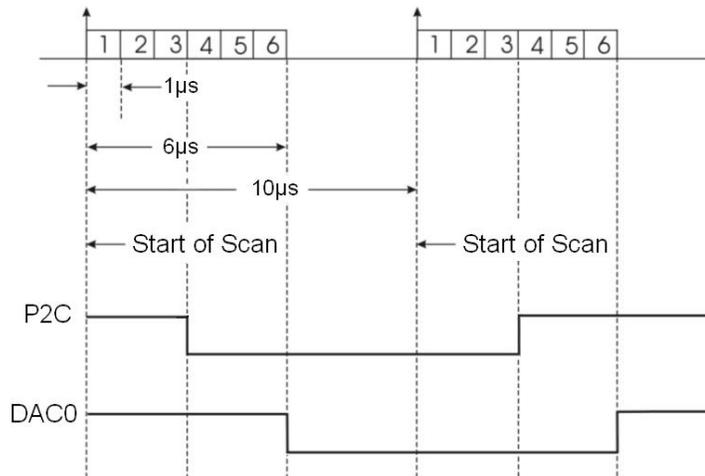
P2C, DAC, or Timer Update Latency

Setpoints allow DACs, timers, or P2C digital outputs to be updated very quickly. Exactly how fast an output can be updated is determined by the following three factors:

- scan rate
- synchronous sampling mode
- type of output to be updated

Example:

We set an acquisition to have a scan rate of 100 kHz. This means each scan period is 10 μ s. Within the scan period we will sample six analog input channels. These are shown in the following figure as Channels 1 through 6. The ADC conversion occurs at the beginning of each channel's 1 μ s time block.



Example of P2C or DAC Latency

If we apply a setpoint on analog input Channel 2, then that setpoint will get evaluated every 10 μ s with respect to the sampled data for Channel 2.

Due to the pipelined architecture of the Analog-to-Digital Converter system, the setpoint cannot be evaluated until 2 μ s after the ADC conversion. In the example above, the P2C digital output port can be updated no sooner than 2 μ s after Channel 2 has been sampled, or 3 μ s after the start of the scan. This 2 μ s delay is due to the pipelined ADC architecture. The setpoint is evaluated 2 μ s after the ADC conversion and then P2C can be updated immediately.

P2C digital outputs can be updated immediately upon setpoint detection. This is not the case for analog outputs, as these incur another 3 μ s delay. This is due to the shifting of the digital data out to the D/A converter which takes 1 μ s, plus the actual conversion time of the D/A converter, i.e., another 2 μ s (worst case). Going back to the above example, if the setpoint for analog input Channel 2 required a DAC update it would occur 5 μ s after the ADC conversion for Channel 2, or 6 μ s after the start of the scan.



When using setpoints to control any of the DAC outputs, increased latencies may occur if attempting to stream data to DACs or pattern digital output at the same time. The increased latency can be as long as the period of the DAC pacer clock. For these reasons, avoid streaming outputs on any DAC or pattern digital output when using setpoints to control DACs.

More Examples of Control Outputs

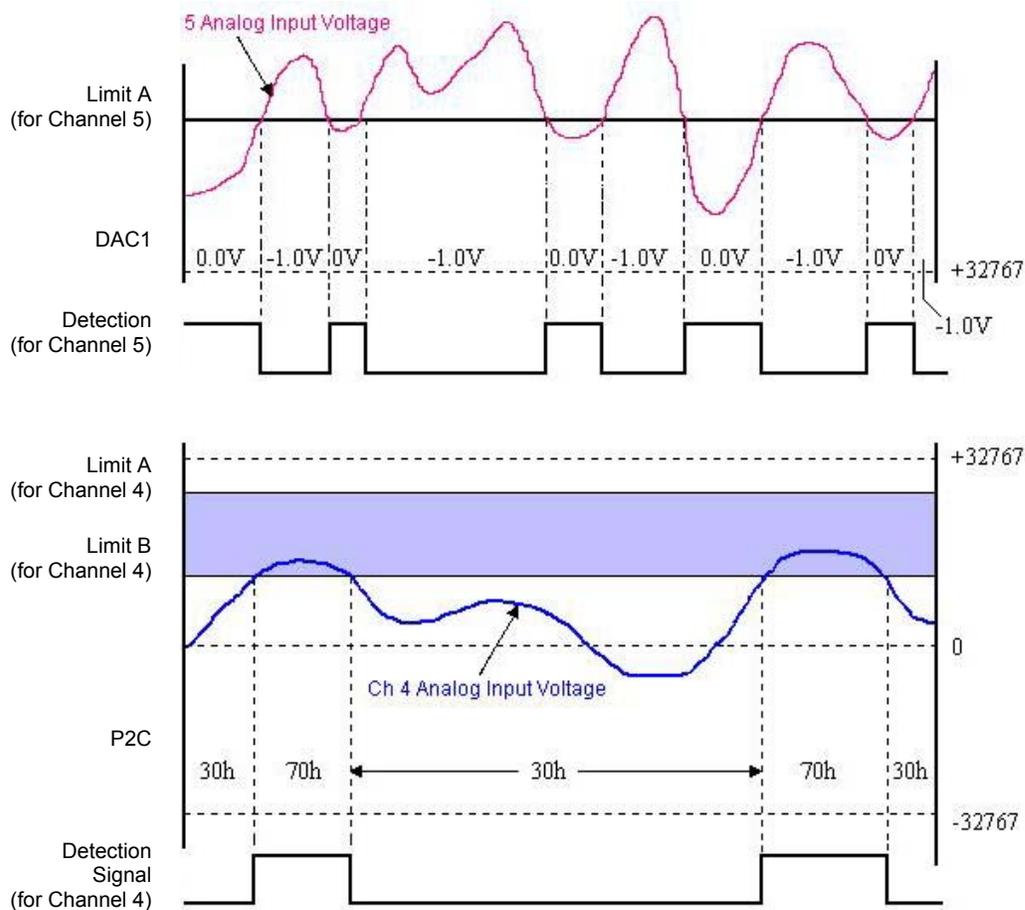
Detection on an Analog Input, DAC and P2C Updates

Update Mode: Update on True and False

Criteria: Ch 5 example: Below Limit; Ch 4 example: Inside Window

In this example Channel 5 has been programmed with reference to one setpoint [Limit A], defining a low limit; and Channel 4 has been programmed with reference to two setpoints [Limits A and B] which define a window for that channel.

Channel	Condition	State of Detect Signal	Action
5	Below Limit A (for Channel 5)	True	When Channel 5 analog input voltage is below the limit A, update DAC1 with Output Value 0.0V.
		False	When the above stated condition is false, update DAC1 with the Output Value of <i>minus</i> 1.0V.
4	Within Window (Between Limit A and Limit B) for Channel 4	True	When Channel 4 analog input voltage is within the window, update P2C with 70h.
		False	When the above stated condition is false (Channel 4 analog input voltage is outside the window) update P2C with 30h.



*Analog Inputs with Setpoints
Update on True and False*

In the example [upper portion of the preceding figure], the setpoint placed on analog Channel 5 updated DAC1 with 0.0V. The update occurred when Channel 5's input was less than the setpoint (Limit A). When the value of Channel 5's input was above setpoint Limit A, the condition of $<A$ was false and DAC1 was then updated with *minus*1.0V.

Control outputs can be programmed on each setpoint. Detection for Channel 4 could be used to update the P2C digital output port with one value (70h in the example) when the analog input voltage is within the shaded region and a different value when the analog input voltage is outside the shaded region (30h in the example).

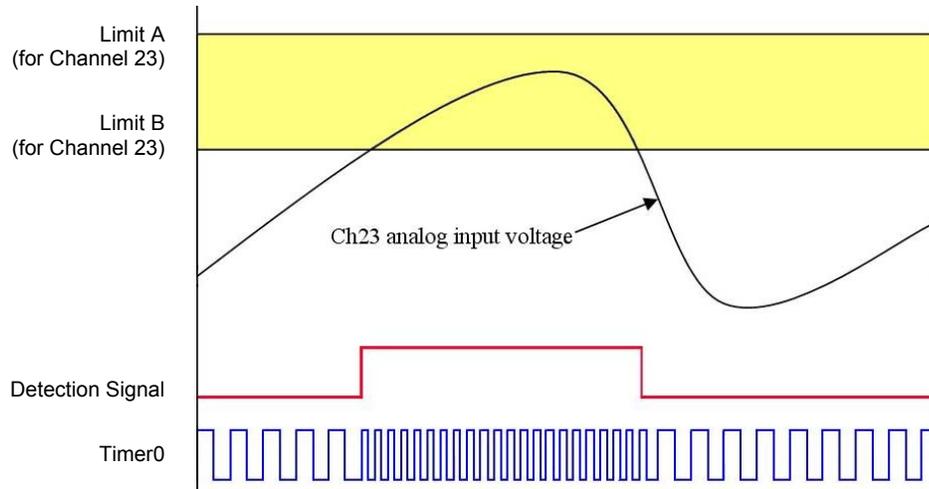
Detection on an Analog Input, Timer Output Updates

Update Mode: Update on True and False

Criteria Used: Inside Window

The figure below shows how a setpoint can be used to update a timer output. Channel 23 is an analog input channel. It could be any analog input channel but in this example it happens to be on a PDQ30 expansion module. A setpoint is applied using *Update on True and False*, with a criteria of *inside-the-window*, where the signal value is inside the window when simultaneously less than Limit A but greater than Limit B.

Whenever the Channel 23 analog input voltage is inside the setpoint window (condition True), timer0 will be updated with one value; and whenever the Channel 23 analog input voltage is outside the setpoint window (condition False) timer0 will be updated with a second output value. An output value of 65535 will stop the timer.



*Updating a Timer Output
Update on True and False*

Using the Hysteresis Function

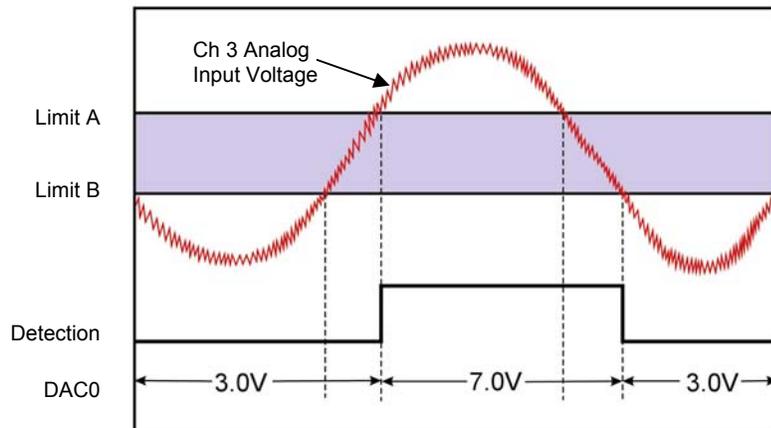
Update Mode: N/A, the Hysteresis option has a forced update built into the function
Criteria Used: window criteria for *above* and *below* the set limits

The figure below shows analog input Channel 3 with a setpoint which defines two 16-bit limits, Limit A (High) and Limit B (Low). These are being applied in the hysteresis mode and DAC Channel 0 will be accordingly.

In this example Channel 3's analog input voltage is being used to update DAC0 as follows:

- **When outside the window, low** (below Limit B) DAC0 is updated with 3.0V. This update will remain in effect until the analog input voltage goes above Limit A.
- **When outside the window, high** (above Limit A) DAC0 is updated with 7.0V. This update will remain in effect until the analog input signal falls below Limit B. At that time we are again outside the limit "low" and the update process repeats itself.

Hysteresis mode can also be done with P2C digital output port, or a timer output, instead of a DAC.



Channel 3 in Hysteresis Mode

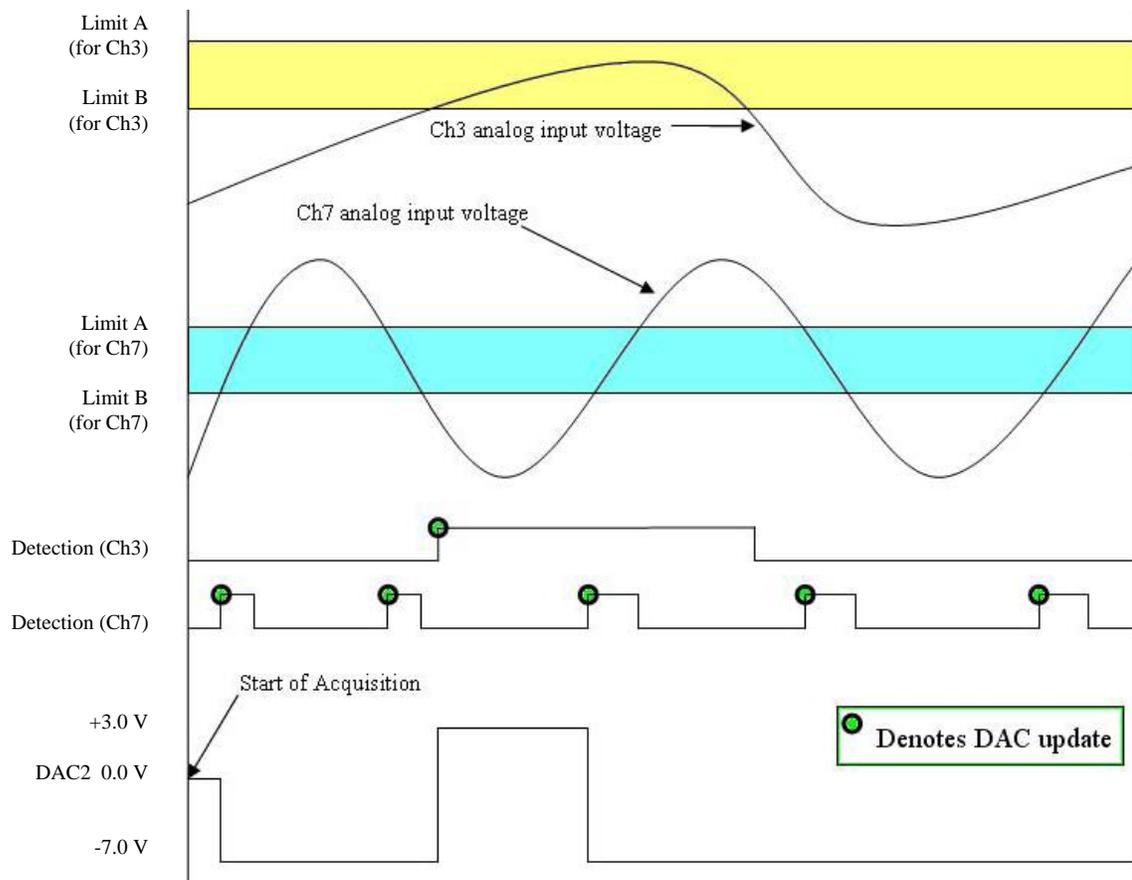
Using Multiple Inputs to Control One DAC Output

Update Mode: Rising Edge, for each of 2 channels

Criteria Used: Inside Window, for each of 2 channels

The figure below shows how multiple inputs can update one output. In the following figure the DAC2 analog output is being updated. Analog input Channel 3 has an *inside-the-window* setpoint applied. Whenever Channel 3's input goes inside the programmed window, DAC2 will be updated with 3.0V.

Analog input Channel 7 also has an *inside-the-window* setpoint applied. Whenever Channel 7's input goes inside the programmed window, DAC2 will be updated with *minus 7.0V*.



*Using Two Criteria to Control an Output**

* The update on *True Only* mode was selected and therefore the updates for DAC2 will only occur when the criteria is met. However, in the above figure we see that there are 2 setpoints acting on one DAC. We can also see that the channel's two criteria can be met during the same scan. When both channel criteria [from the scan] are *True*, then the DAC2 voltage will be associated with the one most recently met.

The Setpoint Status Register

Regardless of which software application you are using with a Personal Daq/3000 Series device, a setpoint status register can be used to check the current state of the 16 possible setpoints. In the register, Setpoint 0 is the least significant bit and Setpoint 15 is the most significant bit. Each setpoint is assigned a value of 0 or 1. 0 indicates that the setpoint criteria is not met, i.e., the condition is false. 1 indicates that the criteria has been met, i.e., the condition is true. Related information is provided in the overview (pages 6-1 and 6-2.)

In the following example, the criteria for setpoints 0, 1, and 4 is satisfied (True); but the criteria for the other 13 setpoints has not been met.

Setpoint #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
True (1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1
False (0)																
	<<< Most Significant Bit								Least Significant Bit >>>							

From the above table we have 10011 binary, or 19 decimal, derived as follows:

Setpoint 0, having a True state, shows “1;” giving us decimal “1.”

Setpoint 1, having a True state, shows “1;” giving us decimal “2.”

Setpoint 4, having a True state, shows “1;” giving us decimal “16.”



For proper operation, the Setpoint Status Register must be the last channel in the scan list.



Notes

Personal Daq/3000 Series Specifications

I/O Comparison Matrix						
Product or System	Analog Input Channels 	Input Ranges	Analog Output Channels 	Digital I/O Channels 	Counter Inputs 	Timer Outputs 
Personal Daq/3000	16SE / 8DE	7	2	24	4	2
Personal Daq/3001	16SE / 8DE	7	4	24	4	2
Personal Daq/3005	16SE / 8DE	7	0	24	4	2
Personal Daq/3000 with PDQ30	64SE / 32DE	7	2	24	4	2
Personal Daq/3001 with PDQ30	64SE / 32DE	7	4	24	4	2
Personal Daq/3005 with PDQ30	64SE / 32DE	7	0	24	4	2

General Specifications

Power Consumption¹

Model	Power Consumption (Typical) ²
/3000	2500 mW
/3001	3000 mW
/3005	2000 mW
/3000 & PDQ30	2900 mW
/3001 & PDQ30	3400 mW
/3005 & PDQ30	2400 mW

¹ The power consumption listed is for a single Personal Daq/3000 Series device, or for a single device connected to a PDQ30 expansion module.

² An optional power adapter (TR-2) will be required if the USB port cannot supply adequate power. USB2 ports are, by USB2 standards, required to supply 2500 mW (nominal at 5V, 500 mA).

Environment:

Operating Temperature: -30 to +70°C; Storage Temperature: -40 to +80°C
Relative Humidity: 0 to 95% non-condensing

Communications: USB2.0 high-speed mode (480 Mbps) if available, otherwise USB1.1 full-speed mode (12 Mbps)

Acquisition Data Buffer: 1 MSample

Vibration: MIL STD 810E Category 1 and 10

Signal I/O Connector: 6 banks of removable screw-terminal blocks

External Power:

Connector: Switchcraft#RAPC-712
Power Range: 6 to 16 VDC (used when USB port supplies insufficient power, or when an independent power supply is desired)
Over-Voltage: 20 V for 10 seconds, max.

Expansion Connector: 25-pin DSUB, female

Physical Attributes:

Dimensions: 269 mm W x 92 mm D x 45 mm H (10.6" x 3.6" x 1.6")
Weight: 431 g (0.95 lbs)

Analog Inputs

Channels: 16 single-ended or 8 differential. Programmable on a per-channel basis as single-ended or differential.

Expansion: An additional 48 analog inputs per module via optional PDQ30 module. Expansion channel features are identical to those of the main channels.

Expansion Connector: 25-pin DSUB, female

Over-Voltage Protection: $\pm 30V$ without damage

Voltage Measurement Speed: 1 μs per channel

Ranges: Software or sequencer selectable on a per-channel basis.
 $\pm 10V$, $\pm 5V$, $\pm 2V$, $\pm 1V$, $\pm 0.5V$, $\pm 0.2V$, $\pm 0.1V$

Input Impedance: 10M Ω single-ended; 20M Ω differential

Total Harmonic Distortion: -80 dB, typical for $\pm 10V$ range, 1 kHz fundamental

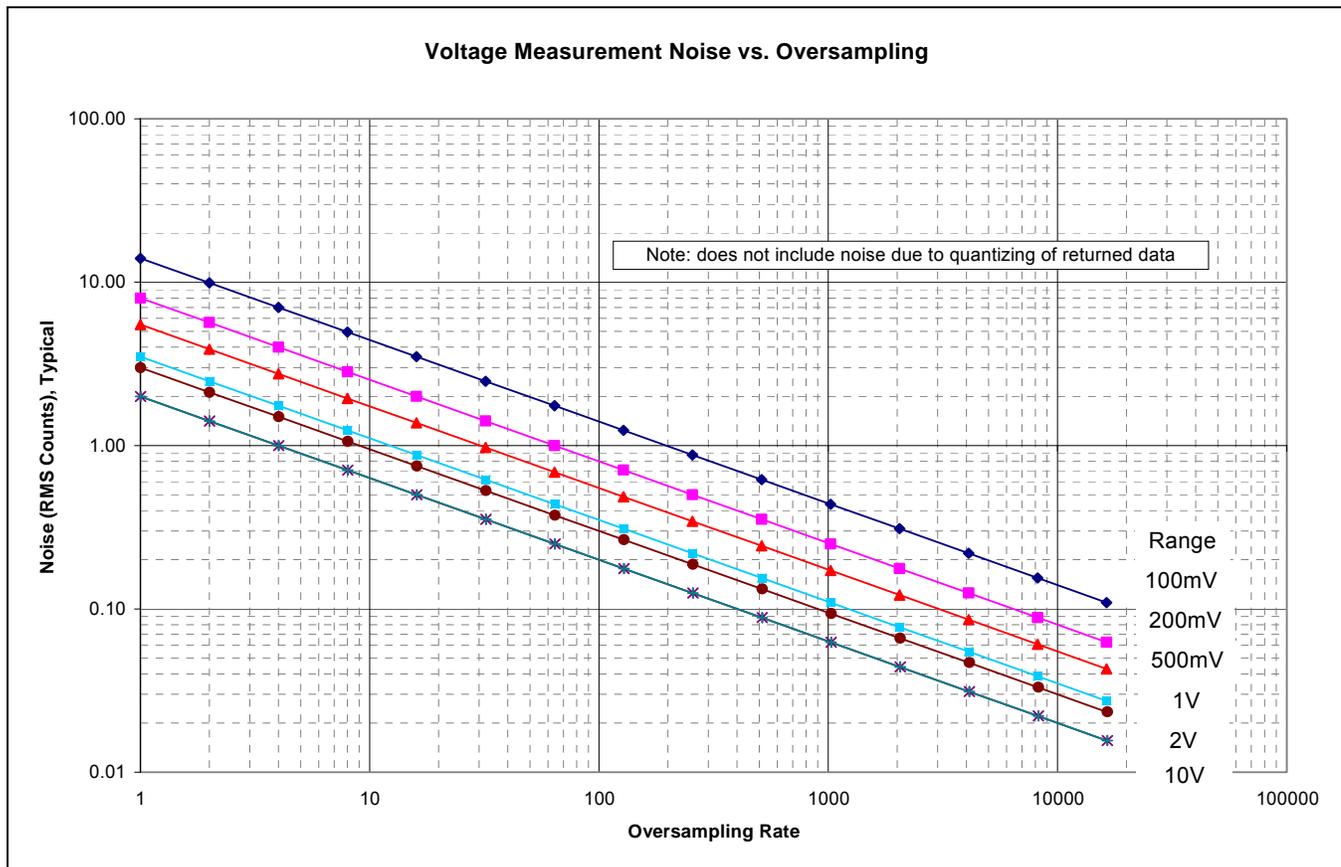
Signal to Noise and Distortion: 72 dB, typical for $\pm 10V$ range, 1 kHz fundamental

Bias Current: 40 pA typical (0°C to 35°C)

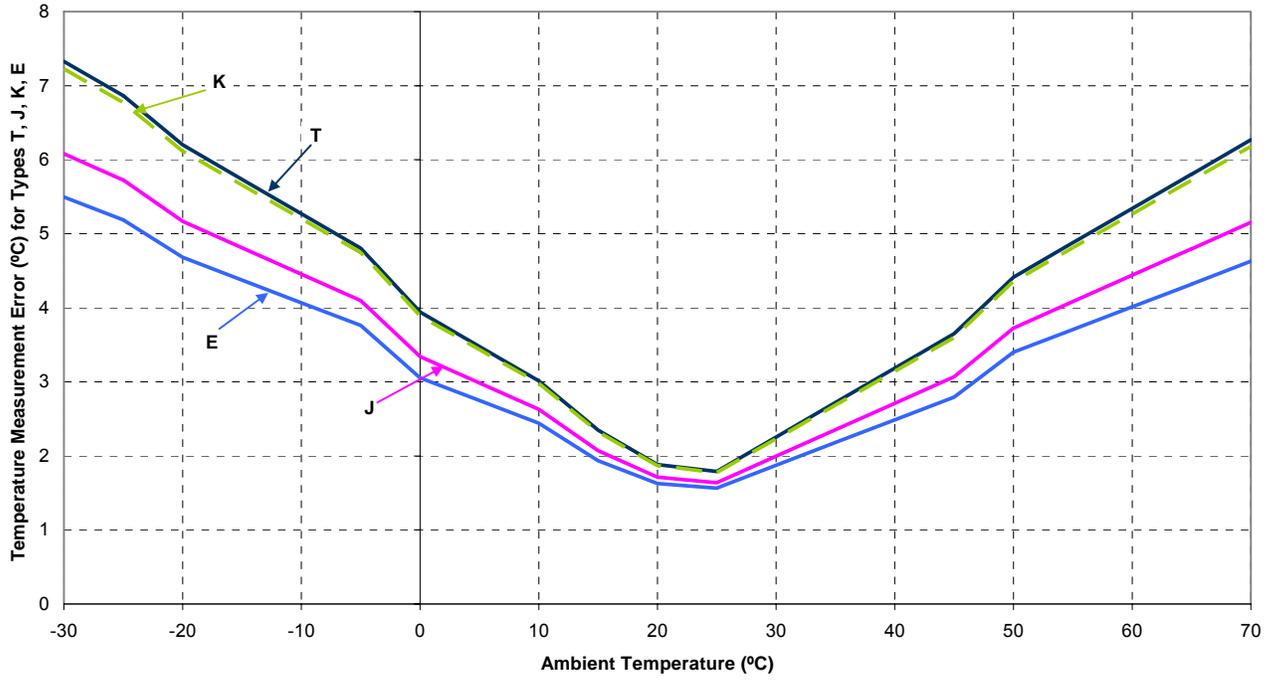
Crosstalk: -75 dB DC to 60 Hz; -65 dB @10 kHz, typical

Common Mode Rejection: -70 dB typical DC to 1 kHz

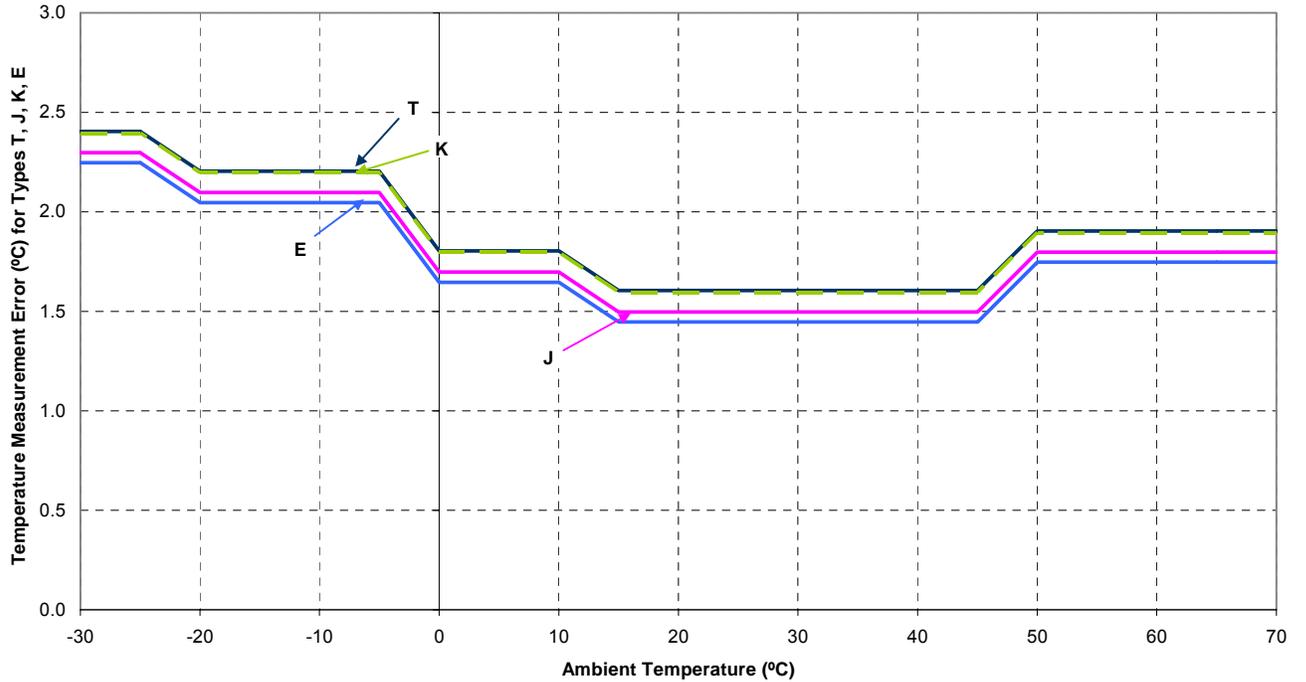
Maximum Usable Input Voltage + Common Mode Voltage	
Ranges	Maximum (CMV + V_{in})
5, 10V	10.5V
0.1, 0.2, 0.5, 1, 2V	6.0V



Worst Case Temperature Measurement Error vs. Personal Daq3000 Ambient Temperature with Thermocouple at 0°C (Excludes Thermocouple Error); AutoZero Disabled; Selected Thermocouple Types: T, J, K, and E



Worst Case Temperature Measurement Error vs. PDaq3000 Ambient Temperature with Thermocouple at 0°C (Excludes Thermocouple Error); AutoZero Enabled; Selected Thermocouple Types: T, J, K, and E



Voltage Range*	Accuracy ±(% Reading + % Range) 23°C ± 10°C, 1 year	Temperature Coefficient ± (ppm of Reading + ppm Range)/°C -30°C to 13°C and 33°C to 70°C	Noise** (cts RMS)
-10V to 10V	0.031% + 0.008%	14 + 8	2.0
-5V to 5V	0.031% + 0.009%	14 + 9	3.0
-2V to 2V	0.031% + 0.010%	14 + 10	2.0
-1V to 1V	0.031% + 0.02%	14 + 12	3.5
-500 mV to 500 mV	0.031% + 0.04%	14 + 18	5.5
-200 mV to 200 mV	0.036% + 0.05%	14 + 12	8.0
-100 mV to 100 mV	0.042% + 0.10%	14 + 18	14.0

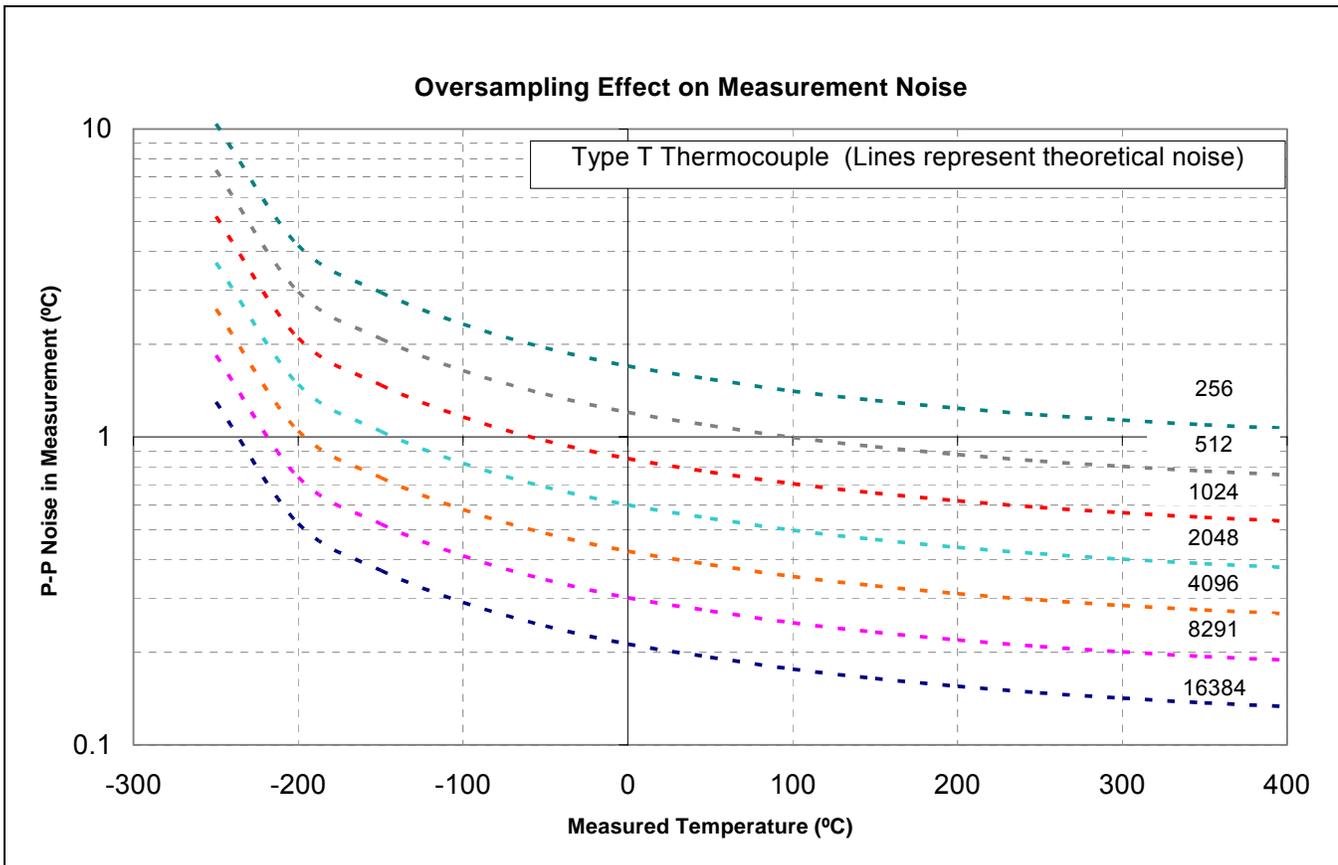
* Specifications assume differential input single-channel scan, 1-MHz scan rate, unfiltered, CMV=0.0V, 30 minute warm-up, exclusive of noise, range is -FS to +FS.

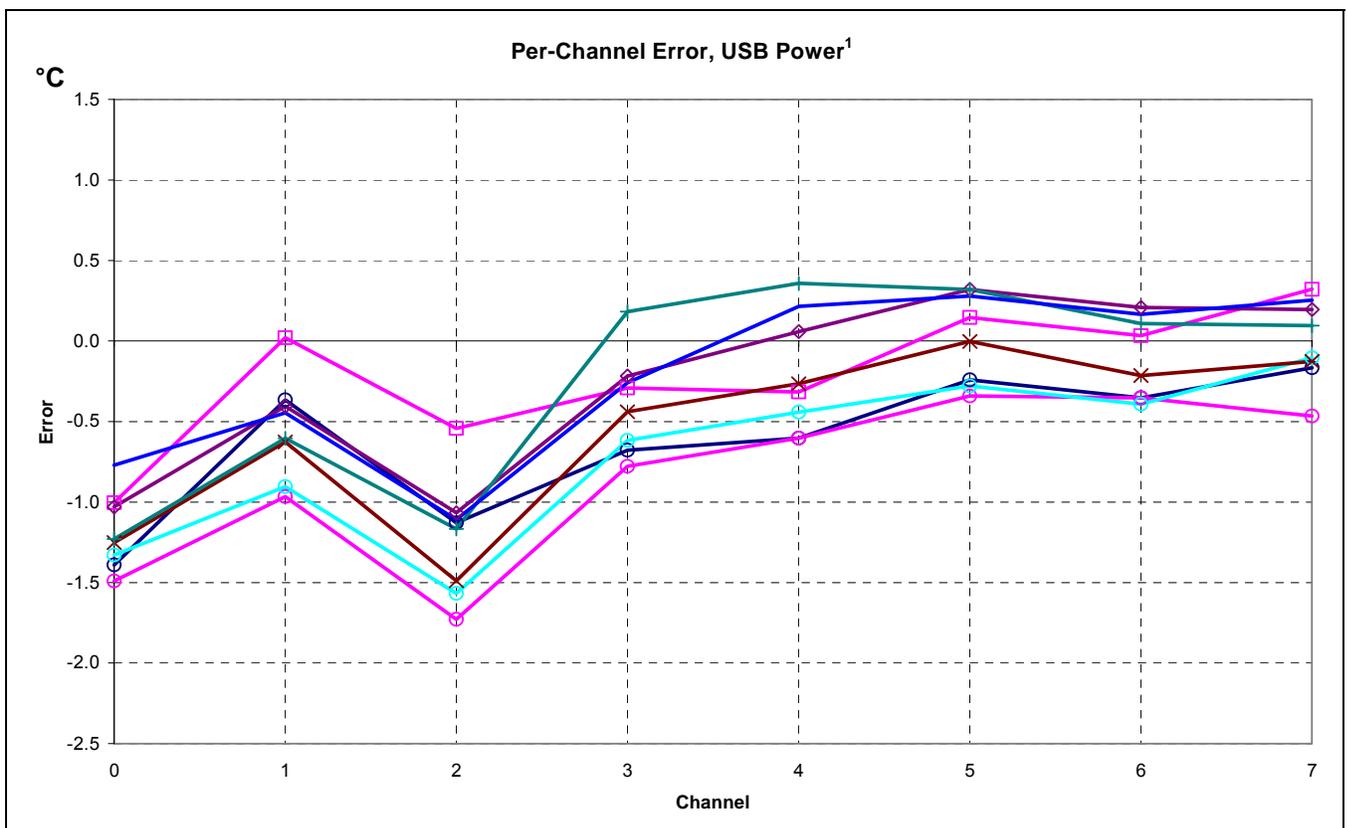
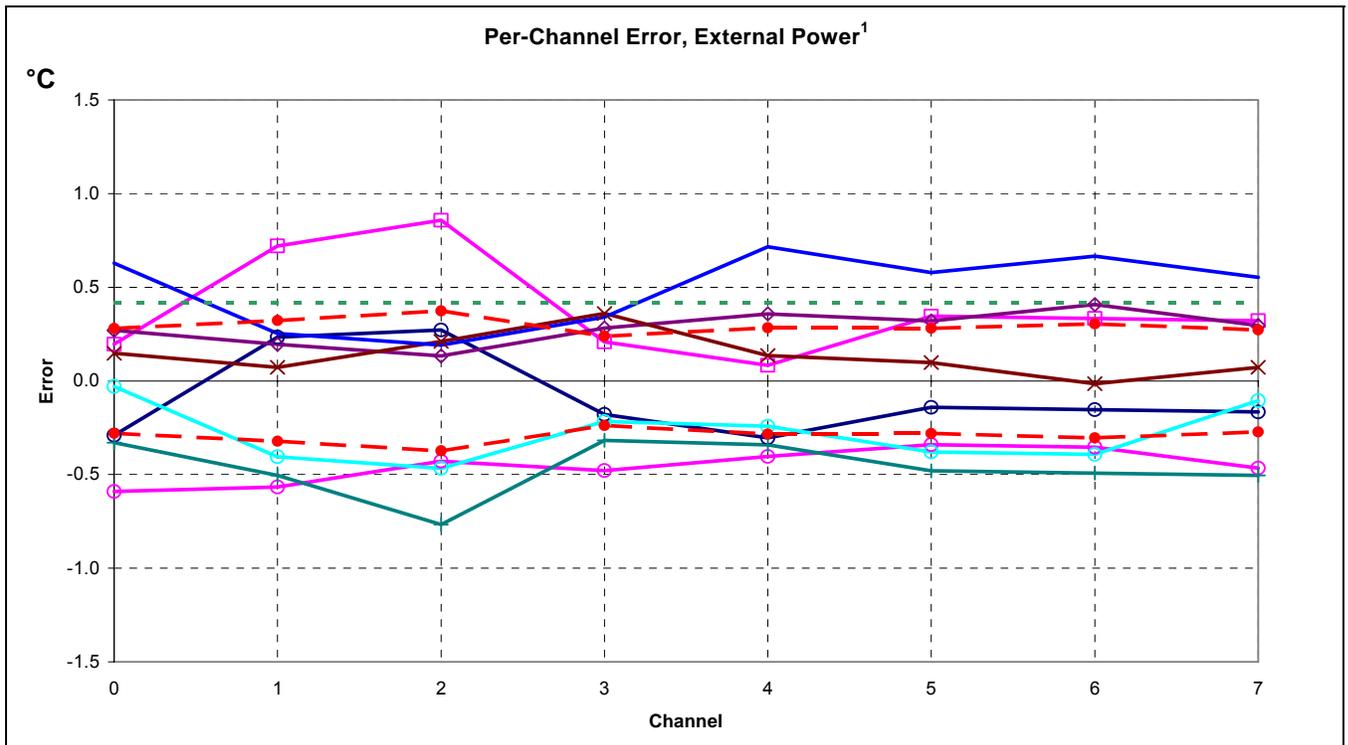
** Noise reflects 10,000 samples at 1-MHz, typical, differential short.

TC Types and Accuracy¹

TC Type	Temperature Range (°C)	Accuracy (±°C)	Noise, Typical (±°C)
J	-200 to +760	1.7	0.2
K	-200 to +1200	1.8	0.2
T	-200 to +400	1.8	0.2
E	-270 to +650	1.7	0.2
R	-50 to +1768	4.8	1.5
S	-50 to +1768	4.7	1.5
N	-270 to +1300	2.7	0.3
B	+300 to +1400	3.0	1.0

¹ Assumes 16384 oversampling applied, CMV = 0.0V, 60 minute warm-up, still environment, and 25°C ambient temperature; excludes thermocouple error; TC_{IN} = 0°C for all types except B (1000°C), TR-2 for External Power.





¹ Typical Performance of 8 Personal Daq/3001 Modules. Assumes 16384 oversampling applied, CMV = 0.0V, 60 minute warm-up, still environment, and 25°C ambient temperature; excludes thermocouple error; TC_{IN} = 0°C

A/D Specifications

Type: Successive approximation

Resolution: 16 bit

Maximum Sample Rate: 1 MHz

Nonlinearity (Integral): ± 2 LSB maximum

Nonlinearity (Differential): ± 1 LSB maximum

Input Sequencer

Analog, digital, and counter inputs can be scanned synchronously based on either an internal programmable timer, or an external clock source. Analog and digital outputs can be synchronized to either of these clocks.

Scan Clock Sources: 2

Note: The maximum scan clock rate is the inverse of the minimum scan period. The minimum scan period is equal to $1\mu\text{s}$ times the number of analog channels. If a scan contains only digital channels then the minimum scan period is 250 ns.

1. Internal, programmable

Analog Channels from $1\mu\text{s}$ to 19 hours in 20.83 ns steps

Digital Channels and Counters from 250 ns to 19 hours in 20.83 ns steps

2. External, TTL level input

Analog Channels down to $1\mu\text{s}$ minimum

Digital Channels and Counters down to 250 ns minimum

Programmable Parameters per Scan: Channel (random order), gain

Depth: 512 locations

On-module Channel-to-Channel Scan Rate:

Analog: 1 MHz maximum

Digital: 4 MHz if no analog channels are enabled, 1 MHz with analog channels enabled

External Acquisition Scan Clock Input

Maximum rate: 1.0 MHz

Clock Signal Range: Logical zero 0V to 0.8V; Logical one 2.4V to 5.0V

Minimum pulse width: 50 ns high, 50 ns low

Triggering

Trigger Sources: 7, individually selectable for starting and stopping an acquisition. Stop acquisition can occur on a different channel than start acquisition; stop acquisition can be triggered via modes 2, 4, 5, or 6 described below.

- 1. Single-Channel Analog Hardware Trigger:** Any analog input channel can be software programmed as the analog trigger channel, including any of the analog expansion channels.
Input Signal Range: -10 to +10V max
Trigger Level: Programmable; 12-bit resolution
Hysteresis: Programmable; 12-bit resolution
Latency: 350 ns typical, 1.3 μ s max
Accuracy: $\pm 0.5\%$ of reading, ± 2 mV offset
Noise: 2 mV RMS
- 2. Single-Channel Analog Software Trigger:** Any analog input channel, including any of the analog expansion channels, can be selected as the software trigger channel. If the trigger channel involves a calculation, such as temperature, then the driver automatically compensates for the delay required to obtain the reading, resulting in a maximum latency of one scan period.
Input Signal Range: Anywhere within the range of the selected trigger channel
Trigger Level: Programmable; 16-bit resolution, including "window triggering"
Latency: One scan period max
- 3. Single-Channel Digital Trigger:** A separate digital input is provided for digital triggering.
Input Signal Range: -15V to +15V
Trigger Level: TTL
Minimum Pulse Width: 50 ns high; 50 ns low
Latency: 100 ns typical, 1.1 μ s max
- 4. Digital Pattern Trigger:** 8 or 16-bit pattern triggering on any of the digital input ports. Programmable for trigger on equal, above, below, or within/outside of a window. Individual bits can be masked for "don't care" condition.
Latency: One scan period max
- 5. Counter/Totalizer Trigger:** Counter/totalizer inputs can trigger an acquisition. User can select to trigger on a frequency or on total counts that are equal, above, below, or within/outside of a window.
Latency: One scan period max
- 6. Software Trigger:** Trigger can be initiated under program control.
- 7. Multi-Channel Triggering:** Up to 16 channels can be used to generate a trigger condition for any combination of analog, digital, or counter inputs. Multiple channels can either be combined in a logical "or" or "and" condition, with hysteresis programmable per channel. Maximum latency in this mode is one scan period.

Analog Outputs **Applicable to Personal Daq/3000 and /3001 only**

Analog output channels are updated synchronously relative to scanned inputs, and clocked from either a Personal Daq/3000 Series internal clock, or an external clock source. Analog outputs can also be updated asynchronously, independent of any other scanning in the system. Streaming from disk or memory is supported, allowing continuous waveform outputs (limited only by available PC system resources).

Channels:

Personal Daq/3000: 2 DAC channels (DAC0, DAC1)

Personal Daq/3001: 4 DAC channels (DAC0, DAC1, DAC2, DAC3)

Resolution: 16 bits

Data Buffer: PC-based memory

Output Voltage Range: $\pm 10V$

Output Current: ± 1 mA; sourcing more current (1 to 10 mA) may require a TR-2 power adapter option.

Offset Error: $\pm 0.0045V$ maximum

Digital Feedthrough: < 10 mV when updated

DAC Analog Glitch: < 12 mV typical at major carry

Gain Error: $\pm 0.01\%$

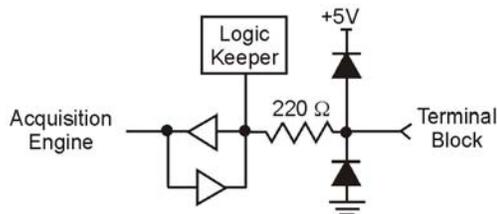
Update Rate: 1 MHz maximum, 19 hours minimum (no minimum with external clock); resolution: 20.83 ns

Settling Time: 2 μs maximum to rated accuracy

Clock Sources: 4 programmable

1. Internal D/A clock, independent of scanning input clock
2. Internal scanning input clock
3. External D/A input clock, independent of external scanning input clock
4. External scanning input clock

Digital I/O



One Digital I/O Channel, Typical

Channels: 24

Ports: 3 x 8-bit. Each port is programmable as input or output.

Input Scanning Modes: 2 programmable

1. Asynchronous, under program control at any time relative to input scanning
2. Synchronous with input scanning

Input Characteristics: 220 Ω series resistor, 20 pF to common

Logic Keeper Circuit: Holds the logic value to 0 or 1 when there is no external driver.

Input Protection: ± 15 kV ESD clamp diodes

Input Levels:

Low: 0 to 0.8V

High: +2.0V to +5.0V

Output Levels:

Low: $< 0.8V$

High: $> 2.0V$

Output Characteristics: Output 1.0 mA per pin; sourcing more current (1 to 10 mA) may require a TR-2 power adapter option.

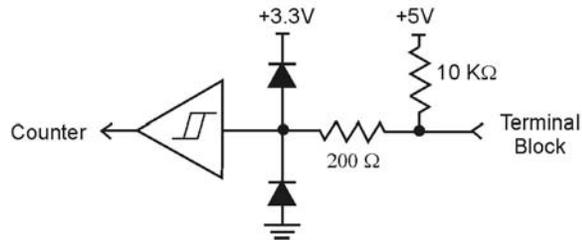
Sampling: 4 MHz, maximum

Update Rate: 4 MHz, maximum, 19 hours minimum (no minimum with external clock); resolution: 20.83 ns

Pattern Generation Output

Two of the 8-bit ports can be configured for 16-bit pattern generation. The pattern can be updated synchronously with an acquisition at up to 4 MHz.

Counters



One Counter Channel, Typical

Each of the four high-speed, 32-bit counter channels can be configured for counter, period, pulse width, time between edges, or multi-axis quadrature encoder modes. Counter inputs can be scanned synchronously along with analog and digital scanned inputs, based on an internal programmable timer, or an external clock source.

Channels: 4 x 32-bit

Input Frequency: 20 MHz maximum

Input Signal Range: -5V to +10V

Input Characteristics: 10 kΩ pull-up, 200Ω series resistor, ±15 kV ESD protection

Trigger Level: TTL

Minimum pulse width: 25 ns high, 25 ns low

Debounce Times: 16 selections from 500 ns to 25.5 ms. Positive or negative edge sensitive. Glitch detect mode or debounce mode.

Time Base Accuracy: 50 ppm (0° to 50°C)

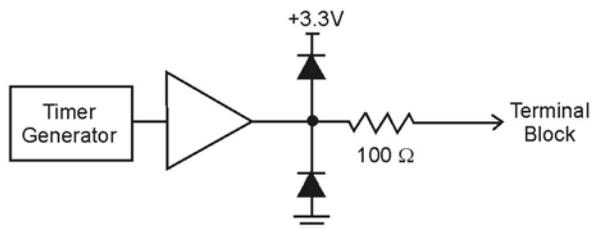
Five Programmable Modes: Counter, Period, Pulswidth, Timing, Encoder

- 1. Counter Mode Options:** Totalize, Clear on Read, Rollover, Stop at all Fs, 16-bit or 32-bit, any other channel can gate or decrement the counter
- 2. Period Mode Options:** Measure x1, x10, x100, or x1000 periods, 16-bit or 32-bit, 4 time bases to choose from (20.83 ns, 208.3 ns, 2.083 μs, 20.83 μs), any other channel can gate the period measurement
- 3. Pulswidth Mode Options:** 16-bit or 32-bit values, 4 time bases to choose from (20.83 ns, 208.3 ns, 2.083 μs, 20.83 μs), any other channel can gate the pulswidth measurement
- 4. Timing Mode Options:** 16-bit or 32-bit values, 4 time bases to choose from (20.83 ns, 208.3 ns, 2.083 μs, 20.83 μs)
- 5. Encoder Mode Options:** x1, x2, x4 options, 16-bit or 32-bit values, Z-channel clearing of the counter, any other channel can gate the counter

Multi-axis Quadrature Encoder Inputs:

- o 1 channel with A (phase), B (phase), and Z (index)
- o 2 channel with A (phase) and B (phase)
- o x1, x2, and x4 count modes
- o Single-ended TTL

Frequency/Pulse Generators



One Timer Channel, Typical

Channels: 2 x 16-bit

Output Waveform: Square wave

Output Rate: 1 MHz base rate divided by 1 to 65535 (programmable)

High Level Output Voltage: 2.0V minimum @ -1.0 mA, 2.9V minimum @ -400 μ A

Low Level Output Voltage: 0.4V maximum @ 400 μ A

Software

DaqViewXL/Plus DaqView add-on for seamless execution with Microsoft Excel's tool palette

DaqView/Pro DaqView add-on includes all of the features of DaqViewXL/Plus, plus frequency-domain analysis

DASyLab Icon-based data acquisition, graphics, control, and analysis software

PDQ30 Specifications

General

Operating Temperature: -30° to +70°C
Storage Temperature: -40° to +80°C
Power: Supplied by DaqBoard/3000 Series or Personal Daq/3000 Series; 400 mW (max)
Relative Humidity: 0 to 95%, non-condensing
Vibration: MIL STD 810E, category 1 and 10
Communications Connector: 25 pin DSUB
Signal I/O Connector: Six removable screw-terminal blocks (12 connections each)
Dimensions: 269mm W x 92mm D x 45 mm H: (10.6" x 3.6" x 1.6")
Weight: 400g (0.88 lbs)

Analog Inputs

Channels: 48 single-ended inputs; or 24 channels differential inputs
Voltage Measurement Speed: 1µs per channel
Ranges: ±10V, ±5V, ±2V, ±1V, ±500mV, ±200mV, ±100mV, universal thermocouple.
 Software or sequencer selectable on a per-channel basis
Total Harmonic Distortion: -80dB typical for ±10V range, 1 kHz fundamental
Signal to Noise and Distortion: 72dB typical for ±10V range, 1 kHz fundamental
Input Impedance: 10M Ohm (single-ended); 20M Ohm (differential)
Bias Current: 40 pA typical (0 to 35°C)
Over-Voltage Protection: ±30V
Crosstalk: -75 dB DC to 60 Hz; -65 dB @ 10 kHz, typical

Voltage Range*	Accuracy ±(% Reading + % Range) 23°C ± 10°C, 1 year	Temperature Coefficient ± (ppm of Reading + ppm Range)/°C -30°C to 13°C and 33°C to 70°C	Noise** (cts RMS)
-10V to 10V	0.031% + 0.008%	14 + 8	2.0
-5V to 5V	0.031% + 0.009%	14 + 9	3.0
-2V to 2V	0.031% + 0.010%	14 + 10	2.0
-1V to 1V	0.031% + 0.02%	14 + 12	3.5
-500 mV to 500 mV	0.031% + 0.04%	14 + 18	5.5
-200 mV to 200 mV	0.036% + 0.05%	14 + 12	8.0
-100 mV to 100 mV	0.042% + 0.10%	14 + 18	14.0

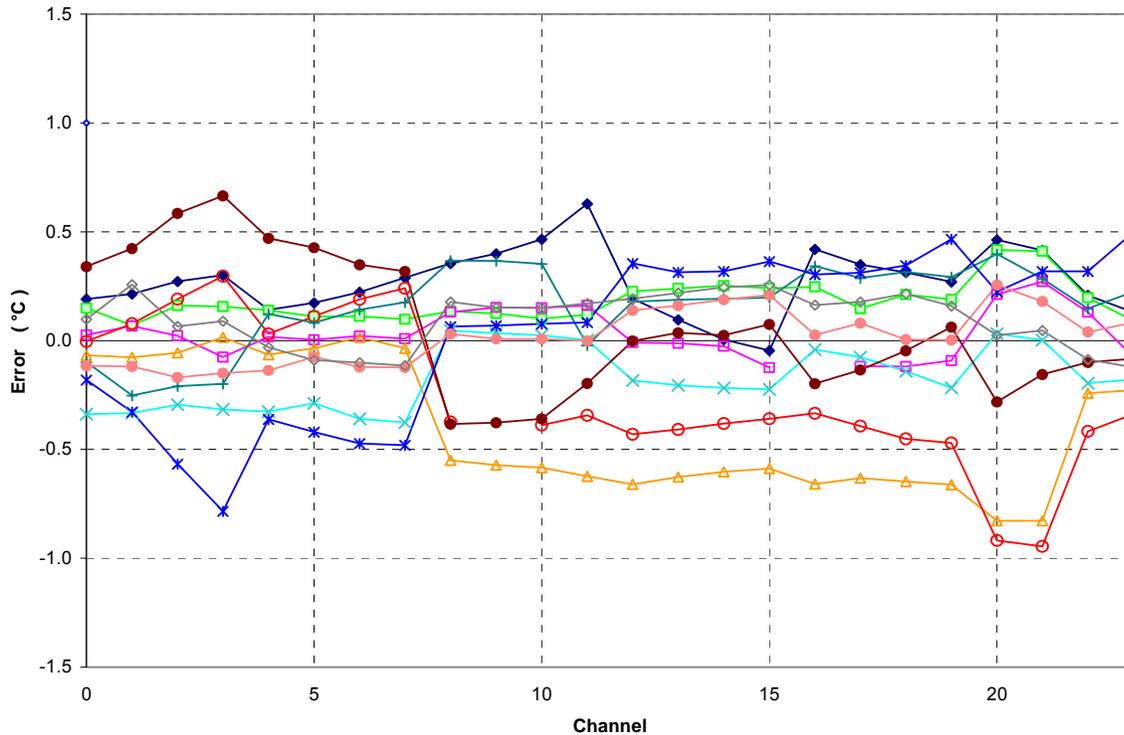
* Specifications assume differential input single channel scan, 1-MHz scan rate, unfiltered, CMV=0.0V, 30 minute warm-up; exclusive of noise, range -FS to +FS.

** Noise reflects 10,000 samples at 1-MHz, typical, differential short

TC Types and Accuracy ¹				
TC	Temp Range (°C)		Accuracy (±°C)	Noise (±°C)
J	-200	to +760	1.7	0.2
K	-200	to +1200	1.8	0.2
T	-200	to +400	1.8	0.2
E	-270	to +650	1.7	0.2
R	-50	to +1768	4.8	1.5
S	-50	to +1768	4.7	1.5
N	-270	to +1300	2.7	0.3
B	+300	to +1400	3.0	1.0

¹ Assumes 16384 oversampling applied, CMV = 0.0V, 60 minute warm-up, still environment, and 25°C ambient temperature; excludes thermocouple error; TC_{IN} = 0°C for all types except B (1000°C), TR-2 for External Power.

PDQ30 Type T Thermocouple
Typical Performance of 12 PDQ30 Units; 0°C (Note 1)



Note 1: Assumes 16384 oversampling applied, CMV = 0.0V, 60 minute warm-up, still environment, and 25°C ambient temperature. Excludes thermocouple error. $TC_{IN} = 0.0\text{ }^{\circ}\text{C}$

Accessories and Cables

PDQ10	DIN-rail mounting adapter.
PDQ11	Powered, 4-port, USB hub with 1 USB cable
PDQ12	USB extension cable (16 ft.), requires TR-2 when used with Personal Daq/3000 Series
PDQ30	Adds 48 SE [or 24 DE] channels to a Personal Daq/3000 Series module. Characteristics of the expansion channels are identical to those of the main channels. PDQ30 can connect directly to a 3000 Series module's DB25 connector, or connect via a CA-96 cable.
CA-96	DB25 male to DB25 female cable; links Personal Daq/3000 Series device to PDQ30 (2 ft.)
CA-179-1	USB cable (1 m)
CA-179-3	USB cable (3 m)
CA-179-5	USB cable (5 m)
CN-153-12	Removable screw-terminal block. 1 block, 12 connections.
TR-2	External power supply. 120VAC to 9VDC, 1A

Signal Modes A-1**Connecting Thermocouples to Screw-Terminal Blocks A-2**

Shielding A-3

TC Common Mode A-3

Cold Junction Compensation Techniques A-4

System Noise A-5

Averaging A-5

Analog Filtering A-5

Input and Source Impedance A-5

Crosstalk A-5

Oversampling and Line Cycle Rejection A-6

Signal Modes

Personal Daq/3000 units can make use of single-ended mode, or differential modes. Mode selection is made in software.

Single-ended mode refers to a mode, or circuit set-up, in which a voltage is measured between 1 signal line and common ground voltage (Analog Common, or A_{COM}). The measured voltage may be shared with other channels. The advantage of a single-ended *non-differential* mode [over differential mode] is that it provides for a higher channel count, for example: 16 channels instead of 8.

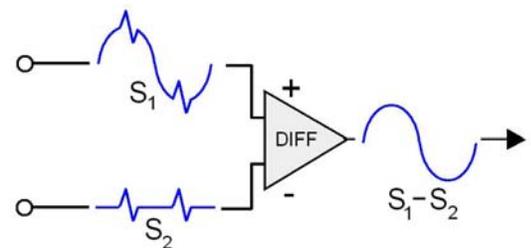


In Personal Daq/3000 applications, thermocouples should never be connected single-ended. Doing so can result in noise and false readings.

Differential mode refers to a mode, or circuit set-up, in which a voltage is measured between two signal lines. The measured differential voltage is used for a single channel. An advantage of using differential inputs is that they reduce signal errors and the induction of noise resulting from ground current. The following illustration is an example of how noise is reduced, or canceled-out, when using the differential mode.

In the schematic, voltage signal S_2 is subtracted from signal S_1 , resulting in the output signal shown. Noise spikes with *the same polarity, phase, and magnitude in each input signal* cancel out—resulting in a clean differential signal ($S_1 - S_2$).

In the schematic, signals S_1 and S_2 are shown in-phase; however, even if these signals were out of phase, the noise in each (indicated by jagged lines) would still have the same magnitude, phase, and polarity. For that reason, they would still cancel out.



Noise Reduction in Differential Mode



Differential signal hookups do not provide isolation or any kind of circuit protection.

Resolution: An analog-to-digital converter (ADC) converts an analog voltage to a digital number. The digital number represents the input voltage in discrete steps with finite resolution. ADC resolution is determined by the number of bits that represent the digital number. An n -bit ADC has a resolution of 1 part in 2^n . Thus, 12 and 16 bit resolutions are as follows:

- 12-bit resolution: 1 part in 4096 (2^{12}), corresponding to 2.44 mV in a 10 V range.
- 16-bit resolution: 1 part in 65,536 (2^{16}), corresponding to 0.153 mV in a 10 V range.

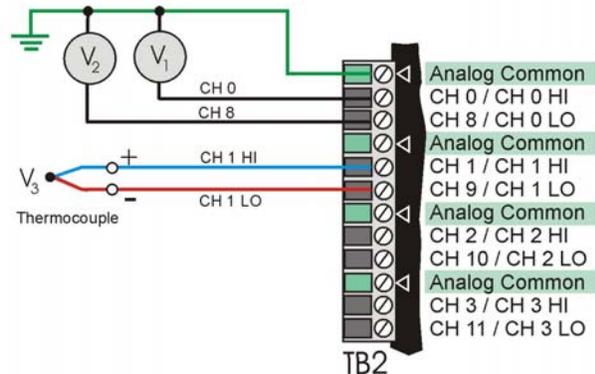
Connecting Thermocouples to Screw Terminal Blocks

Personal Daq/3000 Series modules can measure 16 channels of voltage in *single-ended mode*, 8 channels of voltage in *differential mode*, or 8 channels of temperature in *differential mode*. You can, of course, mix signal types, for example have some channels connected to thermocouples and others connected to voltage signals.

Thermocouple wires are to be connected in differential mode only.

Differential connection is made as follows:

- the red thermocouple wire connects to the channel's Low (L) connector.
- the other color wire connects to the channel's High (H) connector.



Personal Daq/3000 Series and PDQ30 devices do not have open thermocouple detection.

Single-Ended (V1 and V2) and Differential (V3) Connections to Analog Input Channels

Thermocouple wire is standardized, color-coded, and polarized, as noted in the following table.

Thermocouple Standards			
T/C Type	(+) Lead to Channel High	(-) Lead to Channel Low	
J	White	Red	
K	Yellow	Red	
T	Blue	Red	
E	Violet	Red	
N28	Orange	Red	
N14	Orange	Red	
S	Black	Red	
R	Black	Red	
B	Gray	Red	

Thermocouples output very small voltages and long thermocouple leads can pick up a large amount of noise. If desired, noise reduction can be achieved through the use of shielded thermocouples and/or averaging.



You can minimize the effect of noise by employing one or more of the following practices. Using all three is best.

- Use shielded thermocouples** (see *Shielding*, page A-3)
- Average readings** (see *Averaging*, page A-5)
- Route thermocouple wires away from others.** Wires adjacent or close to TC wires may introduce noise into the TC wires. For example, you should never route TC wires in a conduit that is being used for mains or motor drive power. Such practices could introduce a great deal of signal noise.

Shielding

Using shielded TC wire with the shield connected to analog common will result in further noise reduction. Personal Daq/3000 Series modules have one analog common screw-terminal connection for every 2 analog SE channel connections. You can connect the shield of a shielded thermocouple to one of the analog common terminals. When this connection is made the shield at the other end of the thermocouple is to be left unconnected.



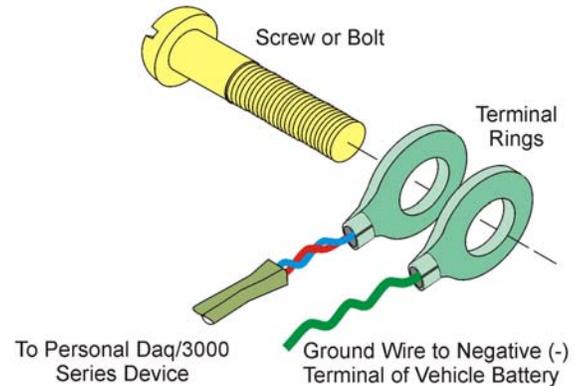
If a thermocouple shield is connected to the Personal Daq/3000 module, leave the shield unconnected at the other end of the thermocouple. Connecting the shield to common at both ends will result in a ground loop.

TC Common Mode

The maximum common-mode voltage for a Personal Daq/3000 Series module is ± 10 volts. Common-mode voltage is the DC or AC voltage signal that is applied equally to both sides of a differential input. Since thermocouples are measured using the 100 mV range, their maximum common mode voltage is ± 6 volts.

If a thermocouple is connected directly to a component in the vehicle at a potential that is over the maximum common-mode voltage, then very noisy or incorrect readings will be seen. Thermocouple connections that are made directly to the alternator or engine block may also result in high noise. Two methods of reducing noise are:

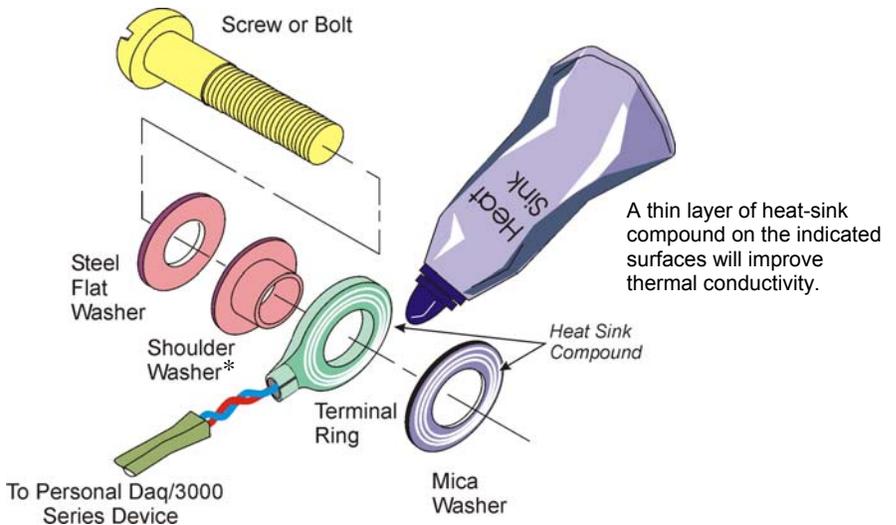
- Run a ground line from the screw (or bolt), as indicated in the following figure.
- Isolate the thermocouple leads with a set of washers, one of which is electrically insulating (such as mica), as indicated in the second figure.



Running a Ground Wire to the Battery's Negative Terminal

The length of the insulating shoulder washer's hub must not exceed the combined thickness of the terminal ring and mica washer.

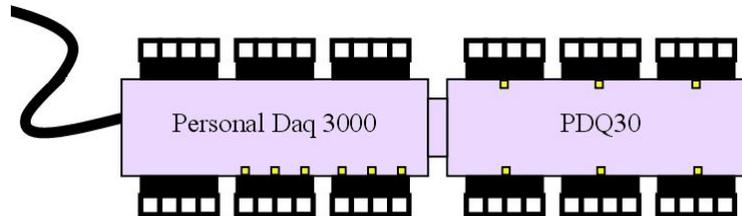
* The insulating shoulder washer is non-metallic. It is made of insulating material, such as plastic.



Using a Washer Set and Heat Sink to Isolate the Thermocouple

Cold Junction Compensation Techniques

The Personal Daq/3000 can measure up to 8 channels of temperature; and the PDQ30 can measure up to 24 channels of temperature. Both units employ thermistors to measure the junction temperature (at the terminal block) for each thermocouple connection. These thermistors are inside the unit, just behind the mating terminal block connector on the internal circuit board. The actual junction is outside the unit and therefore there is some amount of error in the thermistor's ability to measure the actual junction temperature.



Since the Personal Daq/3000 generates more heat internally, there are more thermistors per terminal block than the PDQ30. The PDQ30 generates little heat. There are three thermistors per terminal block on the Personal Daq/3000 but only one thermistor per terminal block on the PDQ30.

Personal Daq software compensates for the thermal error between the CJC thermistor temperature and the actual junction temperature at the terminal block. The units are profiled under controlled conditions (still air, 25C, 60 minute warm-up, lying on a flat surface) and the thermal error is measured on a per channel basis. This is done for the Personal Daq/3000 and the PDQ30. The per-channel CJC temperature offsets are then stored inside the unit in non-volatile memory, along with the calibration constants.



Tips for Making Accurate Temperature Measurements

- Use as much oversampling as possible. (See section, *Oversampling and Line Cycle Rejection* (page A-6).
- Apply Line Cycle Noise Reduction (See section, *Oversampling and Line Cycle Rejection* (page A-6).
- Make sure the unit has been warmed up for at least 60 minutes, including the installed terminal blocks and thermocouple wires. This allows the unit to thermally stabilize so the CJC thermistors can accurately measure the junction at the terminal block.
- Make sure the environment around the Personal Daq/3000 or PDQ30 is thermally stabilized and ideally around 20C to 30C. If the Personal Daq's ambient temperature is changing due to a local heating or cooling source, then the TC junction temperature may be changing and the CJC thermistor will have a larger error.
- Use small diameter thermocouple wire that is "instrument grade." Small diameter thermocouple wire will have less effect on the thermocouple junction at the terminal block, less heat will be transferred from the ambient environment to the junction.
- Make sure the Personal Daq/3000 or PDQ30 is lying on a flat surface.
- If the unit will have a sustained ambient operating environment outside of the 20C to 30C range, consider autozero mode as a way to reduce the effects of offset drift. Performing a $Y=MX+B$ adjustment at a desired ambient temperature can also be done, make sure the unit has stabilized for at least 60 minutes.
- Be careful to avoid loading down the digital outputs or DAC outputs too heavily (>1 mA). Heavy load-down will cause significant heat generation inside the unit and increase the CJC thermistor error.

System Noise

Laboratory and industrial environments often have multiple sources of electrical noise. An AC power line is a source of 50/60 Hz noise. Heavy equipment (air conditioners, elevators, pumps, etc.) can be a source of noise, particularly when turned on and off. Local radio stations are a source of high-frequency noise, and computers and other electronic equipment can create noise in a multitude of frequency ranges. Thus, an absolute noise-free environment for data acquisition is not realistic. Fortunately, noise-reduction techniques such as averaging, filtering, differential voltage measurement, and shielding are available to reduce noise to an acceptable level.

Averaging

Certain acquisition programs apply *averaging* after several samples have been collected. Depending on the nature of the noise, averaging can reduce noise by the square root of the number of averaged samples. Although averaging can be effective, it suffers from several drawbacks. Noise in measurements only decreases as the square root of the number of measurements — reducing RMS noise significantly may require many samples. Thus, averaging is suited to low-speed applications that can provide many samples.

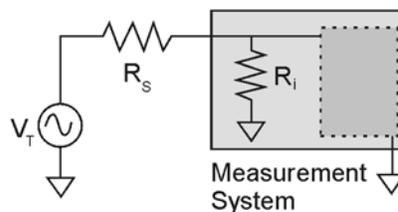
Note: Only random noise is reduced or eliminated by averaging. Averaging does not reduce or eliminate periodic signals. Refer to the section, *Oversampling and Line Cycle Rejection (page A-6)*.

Analog Filtering

A filter is an analog circuit element that attenuates an incoming signal according to its frequency. A low-pass filter attenuates frequencies above the cutoff frequency. Conversely, a high-pass filter attenuates frequencies below the cutoff. As frequency increases beyond the cutoff point, the attenuation of a single-pole, low-pass filter increases slowly. Multi-pole filters provide greater attenuation beyond the cutoff frequency but may introduce phase (time delay) problems that could affect some applications.

Input and Source Impedance

As illustrated in the following figure, input impedance (R_i) of a measurement system combines with the transducer's source impedance (R_s) forming a voltage divider. This divider distorts the voltage being read. The actual voltage read is represented by the equation: $V_{ADC} = V_T \times R_i / (R_s + R_i)$



With input impedance (R_i) of 10 M Ω , which is a realistic value for many measurement systems, a low source impedance (R_s) of less than 100 Ω usually presents no problem. Signals from sources with impedance greater than 100 Ω should have appropriate signal conditioning.

Crosstalk

Crosstalk is a type of noise related to source impedance and capacitance, in which signals from one channel leak into an adjacent channel, resulting in interference or signal distortion. The impact of source impedance and stray capacitance can be estimated by using the following equation.

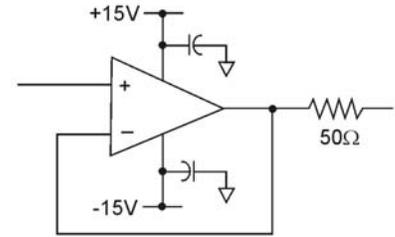
$$T = RC$$

Where T is the time constant, R is the source impedance, and C is the stray capacitance.

High source (transducer) impedance can be a problem in multiplexed A/D systems. When using more than 1 channel, the channel input signals are multiplexed into the A/D. The multiplexer samples one channel and then switches to the next channel. A high-impedance input interacts with the multiplexer's stray capacitance and causes crosstalk and inaccuracies in the A/D sample.

A solution to high source impedance in relation to multiplexers involves the use of buffers. The term buffer has several meanings; but in this case, *buffer* refers to an operational amplifier having high input impedance but very low output impedance. Placing such a buffer on each channel (between the transducer and the multiplexer) prevents the multiplexer's stray capacitance from combining with the high input impedance. This use of a buffer also stops transient signals from propagating backwards from the multiplexer to the transducer.

An example of a buffer is illustrated by the simple op-amp schematic at the right. The op-amp should have a bandwidth between 8MHz and 50MHz, even if the signal being measured is DC. This allows the op-amp to recover quickly from the DaqBoard's input multiplexer charge injection.



Note that characteristics of the op-amp (offset voltage, bias current, etc.) should be chosen with serious consideration for the signal being measured.

Personal Daq/3000 and PDQ30 systems do not have a buffer for each analog input channel, due to power restrictions. Crosstalk is particularly troublesome when measuring high amplitude signals (+/-10V) along with low level signals (+/- 100mV.) All temperature measurements are low level signals that use the +/- 100mV range of the Personal Daq.

If an acquisition's scan group includes both high level signals and low level signals, here are some tips on how to reduce the amount of crosstalk.

- Use as much oversampling as possible.
- Within the scan group, group high level signals together, group low level signals together
- Place a shorted channel in the scan group between the high level signals and the low level signals. The shorted channel should have the same gain as the last high level signal. This may allow for a faster scan rate with less oversampling.

Oversampling and Line Cycle Rejection

The Personal Daq/3000 and PDQ30 allow for oversampling and line cycle rejection to be done. When the units are put into oversampling mode, noise is reduced and ambient 60Hz or 50Hz pick up can be rejected. When enabled, oversampling is adjustable from 2 to 16384. The more oversampling that is done, the less noise present in the readings. Line cycle rejection is just another mode of oversampling where 16384; 8192; 4096; etc. consecutive samples are averaged over one line cycle of 50Hz or 60Hz.

When oversampling is employed it is done for all analog channels in the scan group: voltage, temperature, CJC, autozero, Personal Daq/3000 channels, and PDQ30 channels. Digital channels are not oversampled. Increasing the amount of oversampling will drastically decrease the maximum allowable scan rate. During acquisitions, the system controller reads each of the channel entries in the scan list and measures each channel according to the desired channel number and gain. If oversampling is enabled, the acquisition engine reads each of the channel entries in the scan list and takes multiple consecutive measurements without changing the channel or gain. All consecutive 16-bit measurements are averaged and then returned to the software.

In the case of line cycle rejection, the acquisition engine adjusts the conversion time of the ADC slightly so that 16384; 8192; 4096; etc. samples will fit inside one line cycle of 50 Hz (20ms) or 60Hz (16.666ms). When enabled, line cycle rejection can be applied to all analog channels in the scan list; or it can be applied exclusively to thermocouple channels.

Glossary

Acquisition	A collection of scans acquired at a specified rate as controlled by the sequencer.
Analog	A signal of varying voltage or current that communicates data.
Analog-to-Digital Converter (ADC)	A circuit or device that converts analog values into digital values, such as binary bits, for use in digital computer processing.
API	Application Program Interface. The interface program within the Daq system's driver that includes function calls specific to Daq hardware and can be used with user-written programs (several languages supported).
Bipolar	A range of analog signals with positive and negative values (e.g., -5 to +5 V); see <i>unipolar</i> .
Buffer	<p><i>Buffer</i> refers to a circuit or device that allows a signal to pass through it, while providing isolation, or another function, without altering the signal. <i>Buffer</i> usually refers to:</p> <ul style="list-style-type: none">(a) A device or circuit that allows for the temporary storage of data during data transfers. Such storage can compensate for differences in data flow rates. In a FIFO (First In - First Out) buffer, the data that is stored first is also the first data to leave the buffer.(b) A follower stage used to drive a number of gates without overloading the preceding stage.(c) An amplifier which accepts high source impedance input and results in low source impedance output (effectively, an impedance buffer).
Buffer Amplifier	An amplifier used primarily to match two different impedance points, and isolate one stage from a succeeding stage in order to prevent an undesirable interaction between the two stages. (Also see, <i>Buffer</i>).
Channel	<p>In reference to Daq devices, <i>channel</i> simply refers to a single <i>input</i>, or <i>output</i> entity.</p> <p>In a broader sense, an <i>input channel</i> is a signal path between the transducer at the point of measurement and the data acquisition system. A channel can go through various stages (buffers, multiplexers, or signal conditioning amplifiers and filters). Input channels are periodically sampled for readings.</p> <p>An <i>output channel</i> from a device can be digital or analog. Outputs can vary in a programmed way in response to an input channel signal.</p>
Common mode	Common mode pertains to signals that are identical in amplitude and duration; also can be used in reference to signal components.
Common mode voltage	Common mode voltage refers to a voltage magnitude (referenced to a common point) that is shared by two or more signals. <i>Example:</i> referenced to common, Signal 1 is +5 VDC and Signal 2 is +6 VDC. The common mode voltage for the two signals is +5.5 VDC $[(5 + 6)/2]$.
Crosstalk	An undesired transfer of signals between systems or system components. Crosstalk causes signal interference, more commonly referred to as <i>noise</i> .
Digital	A digital signal is one of discrete value, in contrast to a varying signal. Combinations of binary digits (0s and 1s) represent digital data.
Digital-to-Analog Converter (DAC)	A circuit or device that converts digital values (binary bits), into analog signals.
DIP switch	A DIP switch is a group of miniature switches in a small <i>Dual In-line Package</i> (DIP). Typically, users set these switches to configure their particular application.
Differential mode	The differential mode measures a voltage between 2 signal lines for a single channel. (Also see <i>single-ended mode</i>).

Differential mode voltage	Differential mode voltage refers to a voltage difference between two signals that are referenced to a common point. Example: Signal 1 is +5 VDC referenced to common. Signal 2 is +6 VDC referenced to common. If the +5 VDC signal is used as the reference, the differential mode voltage is +1 VDC (+ 6 VDC - +5 VDC = +1 VDC). If the +6 VDC signal is used as the reference, the differential mode voltage is -1 VDC (+ 5 VDC - +6 VDC = -1 VDC).
ESD	Electrostatic discharge (ESD) is the transfer of an electrostatic charge between bodies having different electrostatic potentials. This transfer occurs during direct contact of the bodies, or when induced by an electrostatic field. ESD energy can damage an integrated circuit (IC).
Excitation	Some transducers [e.g. strain gages, thermistors, and resistance temperature detectors (RTDs)] require a known voltage or current. Typically, the variation of this signal through the transducer corresponds to the condition measured.
Gain	The degree to which an input signal is amplified (or attenuated) to allow greater accuracy and resolution; can be expressed as $\times n$ or $\pm dB$.
Isolation	The arrangement or operation of a circuit so that signals from another circuit or device do not affect the <i>isolated</i> circuit. In reference to Daq devices, <i>isolation</i> usually refers to a separation of the direct link between the signal source and the analog-to-digital converter (ADC). Isolation is necessary when measuring high common-mode voltage.
Linearization	Some transducers produce a voltage in linear proportion to the condition measured. Other transducers (e.g., thermocouples) have a nonlinear response. To convert nonlinear signals into accurate readings requires software to calibrate several points in the range used and then interpolate values between these points.
Multiplexer (MUX)	A device that collects signals from several inputs and outputs them on a single channel.
Range	For the purposes of calculating accuracy, range is equal to the full dynamic input voltage. For example, the full-scale range is 20V for the -10 to +10V range.
Sample (reading)	The value of a signal on a channel at an instant in time. When triggered, the ADC reads the channel and converts the sampled value into a 12- or 16-bit value.
Scan	A series of measurements across a pre-selected sequence of channels.
Sequencer	A programmable device that manages channels and channel-specific settings.
Simultaneous Sample-and-Hold	An operation that gathers samples from multiple channels at the same instant and holds these values until all are sequentially converted to digital values.
Single-ended mode	The single-ended mode measures a voltage between a signal line and a common reference that may be shared with other channels. (Also see <i>differential mode</i>).
Trigger	An event to start a scan or mark an instant during an acquisition. The event can be defined in various ways; e.g., a TTL signal, a specified voltage level in a monitored channel, a button manually or mechanically engaged, a software command, etc. Some applications may use pre- and post-triggers to gather data around an instant or based on signal counts.
TTL	Transistor-Transistor Logic (TTL) is a circuit in which a multiple-emitter transistor has replaced the multiple diode cluster (of the diode-transistor logic circuit); typically used to communicate logic signals at 5 V.
Unipolar	A range of analog signals that is always zero or positive (e.g., 0 to 10 V). Evaluating a signal in the right range (unipolar or bipolar) allows greater resolution by using the full-range of the corresponding digital value. See <i>bipolar</i> .